A 3.6GS/s, 15mW, 50dB SNDR, 28MHz Bandwidth RF ΣΔ ADC with a FoM of 1pJ/bit in 130nm CMOS

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***Abstract*— A 4^{th} order RF LC ΣΔ ADC clocked at 3.6GHz and centered at 900MHz is presented. The simplicity of the ADC architecture results in a significant performance enhancement and power consumption reduction. The ADC, suitable for Software Defined Radio applications, is implemented in a standard 130nm CMOS technology. It achieves a 52dB SFDR and a 50dB SNDR in a 28MHz BW and consumes only 15mW from a 1.2V supply. The Figure of Merit of the ADC is 1.0pJ/bit, which is to date the best reported FoM for an RF ADC. An efficient algorithm for the tuning and calibration of the ΣΔ LC-based loop filter is also presented in this paper.**

I. Introduction

The continuous improvement of both speed and density of digital circuits in CMOS technologies makes it attractive to push most of the chip functionality from the RF and analog domain to the digital domain. In an RF receiver, this means to push the Analog-to-Digital Converter (ADC) near the antenna to achieve what is commonly known as Software Defined Radio (SDR). In SDR receivers, as shown in Fig. 1, most of the analog blocks such as the down-conversion mixer and the channel selection filter are moved to the digital domain. In this case, most of the signal processing is done in the flexible and programmable digital domain.

One of the main challenges in implementing an SDR receiver is the stringent ADC requirements. The ADC must have a large bandwidth and a high dynamic range to be able to deal with the targeted RF band in the presence of strong out-of-band blockers. A promising technique to achieve these ADC specifications is to use a bandpass LC ΣΔ ADC with an RF center frequency. In this paper, we present an efficient realization of an RF bandpass ΣΔ ADC centered at 900MHz.

The ADC is implemented in a standard low-cost CMOS technology and it has a power consumption significantly lower than recent SiGe realizations [1], [2]. Compared with other CMOS implementations [3], [4], the proposed RF bandpass ΣΔ ADC has a simple 4^{th} order architecture with a single-bit quantizer and a minimum number of feedback coefficients [5]. The sampling frequency f_s is equal to 4 times the center frequency f_o. This greatly simplifies the digital single-bit down-conversion mixer and the subsequent decimation filter. Since the sampling frequency of these digital circuits are in the GHz range, having $f_s = 4f_o$, can significantly reduce the power consumption of the overall SDR receiver. In this paper, we also present the calibration algorithm used to tune the center frequency and the quality factor of the loop filter.

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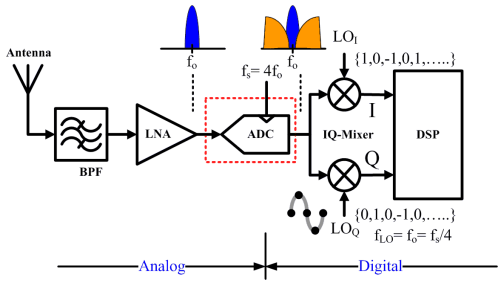


Fig. 1. A Software Defined Radio receiver based on RF ΣΔ ADC.

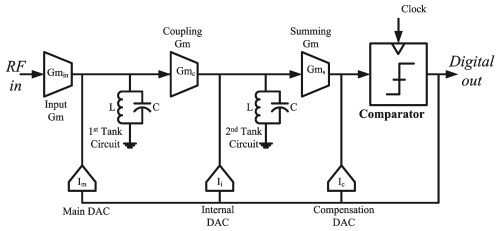


Fig. 2. A simple architecture for a 4^{th} order bandpass ΣΔ ADC. The loop delay is optimized for a minimum number of feedback DAC coefficients.

The paper is organized as follows: section II introduces the ADC architecture, section III discusses the circuit implementation of the main ADC blocks, section IV gives details about the proposed tuning and calibration algorithm, and finally, section V presents the measurement results.

II. Architecture

The bandpass LC ΣΔ ADC is shown in Fig. 2. The system level design of this architecture is based on the DT-to-CT equivalence using feedback FIRDAC described in [6]. The number of FIRDAC coefficients is reduced to one coefficient per LC resonator using the optimization method described in [5]. The main advantage of this architecture is the few number of feedback DAC branches, compared to other LC-based ΣΔ ADC architectures [2]. The architecture simplicity leads to lower thermal noise and power consumption.

The ADC is designed for an input signal centered around 900MHz and it is clocked at 4 times this frequency, i.e the clock frequency is 3.6GHz. This simplifies the down-conversion of the ADC output, as the Local Oscillator (LO) sinusoidal signal becomes a series of $\{1, 0, -1, 0\}$ [7]. The ADC is optimized for an Over-Sampling Ratio (OSR) of 64, which leads to a bandwidth of 28MHz. The OSR is however flexible and it can be changed according to the desired bandwidth and SNR.

As shown in Fig. 2, the loop filter is a 4^{th} order filter based on two cascaded LC tank circuits centered at 900MHz and three transconductors: an input Gm, a coupling Gm and a summing Gm.

The single-bit quantizer, or simply the comparator, is more suitable for RF $\Sigma\Delta$ ADCs, due its inherent linearity. The comparator consists of 4 cascaded latches, not only to avoid the metastability, but also to meet the loop delay required by the architecture [5].

III. Circuit Design

A. Loop Filter

The loop filter is mainly composed of two cascaded LC tank circuits. Each tank circuit consists of a center-tapped inductor and two identical banks of capacitors, as depicted in Fig. 3. The inductor has 6-turns with around $15nH$ inductance and quality factor of about 14. Using two grounded capacitors instead of a single floating capacitor requires more area, but it gives better linearity and simplifies the design of the capacitor bank switches. The capacitor bank has a nominal value of about $3pF$ and can be trimmed in $25fF$ steps to allow for center frequency tuning and calibration.

The low quality factor of the tank circuit is not sufficient to achieve the required noise shaping and it has to be boosted using a cross-coupled transconductor Gm_q that acts a negative resistance and compensates the losses in the tank circuit [2]. The value of the negative resistance can be adjusted by controlling its current which has a nominal value of $600\mu A$ and can be trimmed with a $40\mu A$ step to allow for quality factor calibration. If the current of the negative resistance is increased above a certain limit, oscillation will occur, which can be used in center frequency tuning and calibration, as will be described in section IV.

The input transconductor Gm_{in} circuit is shown in Fig. 4. It is based on a simple differential pair without source degeneration, which is usually used to enhance the linearity [2]. However it was found that source degeneration enhances the Input third-order Intercept Point (IIP3), but can result in a lower Output third-order Intercept Point (OIP3) for the same bias current. The coupling transconductor Gm_c and summing transconductor Gm_s have the same circuit but with a lower current (0.6mA), due to their relaxed specifications compared to Gm_{in}.

B. DAC

The type of the feedback DAC output has to be carefully selected, as it has a direct impact on the ADC performance. Non-

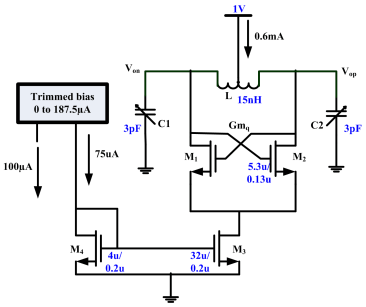


Fig. 3. The LC tank circuit with a tunable center frequency and a tunable quality factor.

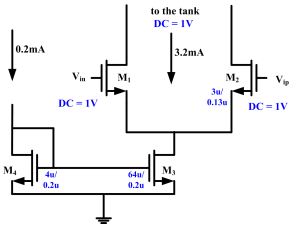


Fig. 4. Input transconductor Gm_{in}.

Return-to-Zero (NRZ) feedback DAC was chosen, because of its simplicity and suitability to high operating frequencies. It also has a better immunity to clock jitter compared to Return-to-Zero (RZ) DAC. Inter-Symbol Interference (ISI) is the main disadvantage of NRZ DAC, however the effect of ISI can be simulated and minimized by proper sizing of the DAC circuit and its driving buffer.

The DAC circuit is a cascode current-steering topology, as shown in Fig. 5. The cascode structure is used to increase the output resistance of the feedback DAC to avoid degrading the tank circuit quality factor. It also provides isolation between the DAC input and output [8].

C. Comparator

As shown in Fig. 6(a), the comparator consists of 4 cascaded latches not only to avoid the metastability, but also to adjust the feedback loop delay to a value that minimizes the number of feedback coefficients [5]. A pre-amplifier is added before the first latch to mitigate the metastability, to reduce the kickback noise and to provide more isolation between the comparator and the loop filter. A buffer stage is added after the last latch

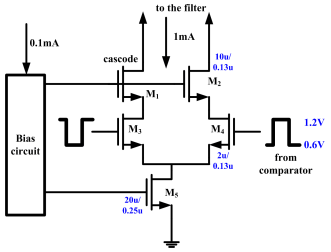
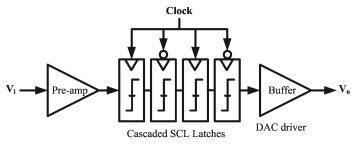
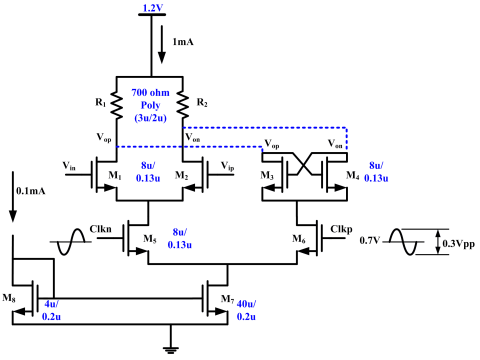


Fig. 5. The cascode current steering DAC circuit.



(a) Comparator architecture.



(b) SCL latch circuit.

Fig. 6. Comparator architecture based on SCL latches.

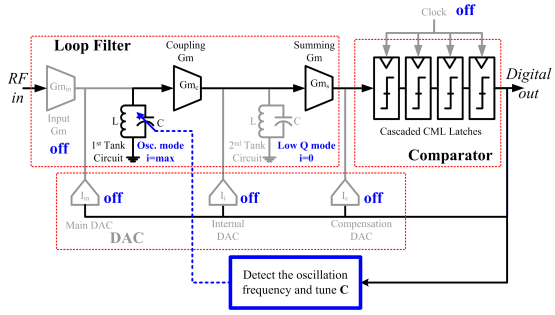


Fig. 7. ADC in calibration mode.

to avoid loading it with the large input capacitance of the feedback DAC.

The Source-Coupled Logic (SCL) latch is used, because it can work at significantly higher speed than the CMOS latch. The design of the SCL latch, shown in Fig. 6(b), is a trade-off between power consumption, voltage swing and high operation speed. The SCL latch is driven by a differential sinusoidal clock of 0.3Vpp and consumes 1mA DC current from the 1.2V supply.

IV. Tuning and Calibration

One of the main issues in CT $\Sigma\Delta$ ADCs is the poor accuracy and the sensitivity to process variations [9]. Trimming is needed to compensate the drift in circuit components to obtain the optimum performance from the ADC. The most important parameters that must be calibrated are the resonance frequency f_o and the quality factor Q of the two LC tank circuits.

An efficient calibration algorithm was suggested in [4] that is based on putting the tank circuit in oscillation mode, then detecting its oscillation frequency.

The calibration procedure, illustrated in Fig. 7, is performed by the following steps:

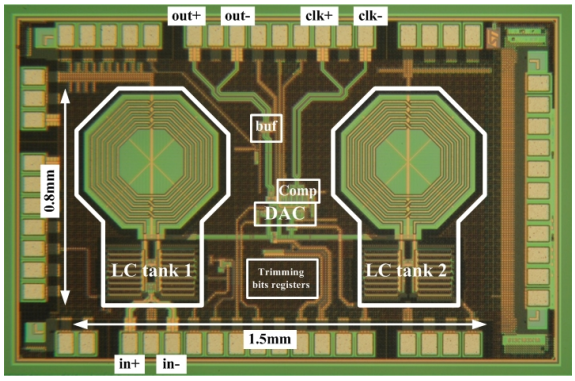


Fig. 8. Chip micrograph.

1) The SCL latches are configured as buffers by deactivating their driving clock.
2) The input signal is disabled by turning off the input transconductor Gm_{in}.
3) The feedback DAC current is turned off.
4) Tank$_1$ is put in oscillation mode by setting its Q-enhancement transconductor Gm_{q1} to its maximum.
5) Tank$_2$ is put in low-Q mode by turning off its Q-enhancement transconductor Gm_{q2}.
6) Capacitor of tank$_1$ C_1 is tuned, till the output frequency is equal to the desired center frequency.
7) Q-enhancement transconductor Gm_{q1} is reduced gradually till oscillation vanishes.
8) Tank$_2$ is calibrated using the same procedure as tank$_1$.

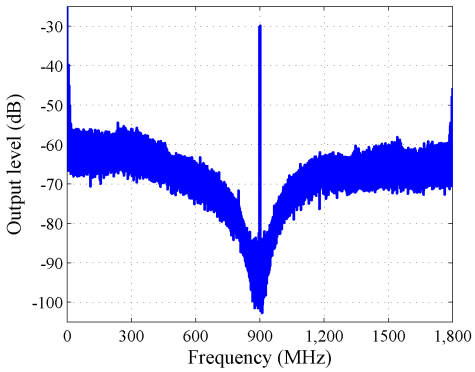
The measurements showed that the digitally-controlled tank circuit covers a wide frequency range ($\sim$ 400MHz) with a fine resolution ($\sim$ 2MHz).

V. Measurement Results

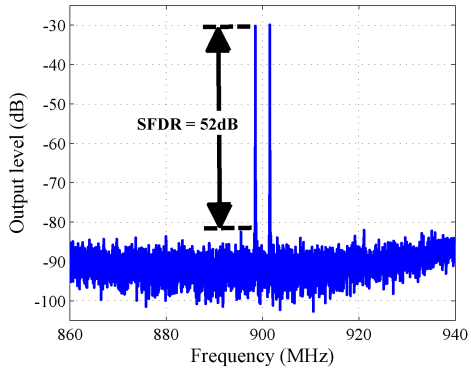
The chip was fabricated in a 130nm CMOS technology. The chip micrograph is shown in Fig. 8. The active area is about $1.2mm^2$. Most of the active area is occupied by the two inductors, the two capacitor banks and the empty space that separates the two inductors.

An IQ vector signal generator was used to generate the input signal centered at 900MHz. The ADC was clocked with a 3.6GHz clock, and the output bit stream was captured using a 40Gs/s digital oscilloscope. FFT is then applied to the captured bit-stream to obtain the spectrum shown in Fig. 9. It can be seen from the figure that the Spurious Free Dynamic Range (SFDR) is about 52dB. The Signal to Noise+Distortion Ratio (SNDR) is then measured for different values of the input signal power, as shown in Fig. 10. The ADC achieves 50dB of SNDR in a 28MHz bandwidth (OSR=64).

Table I compares the achieved performance to some recently published RF $\Sigma\Delta$ ADCs. ADCs are usually compared according to their FoM ($P_{dc}/\left(2\,BW\,2^{ENOB}\right)$). Another FoM proposed in [10] is more adapted to bandpass $\Sigma\Delta$ ADCs (FoM$_{BP}$ = FoM$/\left(1+6f_o/f_s\right)$). Our ADC achieves the best performance for both FoM and FoM$_{BP}$.



(a) Output spectrum of the RF ΣΔ ADC centered at 900MHz.



(b) The band of interest, 80MHz centered at 900MHz.

Fig. 9. Output spectrum obtained from a 2^{17} points FFT and averaged 4 times on the output digital bit stream for a two-tones input signal at 900MHz ± 1.5MHz.

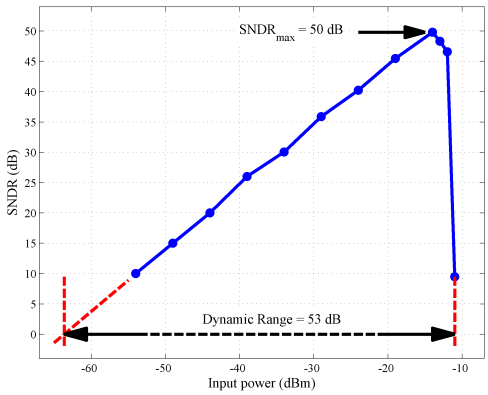


Fig. 10. Measured SNDR versus the input power.

TABLE I
COMPARISON WITH RECENT RF ΣΔ ADCS.

Reference	This work	[4]	[3]	[1]	[2]
Order	4^{th}	4^{th}	2^{nd}	4^{th}	4^{th}
Center frequency	900MHz	2.4GHz	2.4GHz	2GHz	950MHz
Sampling frequency	3.6GHz	6.1GHz	3.2GHz	40GHz	3.8GHz
SNDR	50dB	40dB	34dB	55dB	59dB
Bandwidth	28MHz	80MHz	25MHz	60MHz	1MHz
Power consumption	15mW	53mW	26mW	1.6W	75mW
Technology	CMOS 130nm	CMOS 40nm	CMOS 130nm	SiGe 130nm	SiGe 250nm
FoM (pJ/bit)	1.0	3.6	12.7	20.5	51.5
FoM_{BP} (pJ/bit)	0.4	1.1	2.3	15.8	20.6
$f_s = 4f_o$	Yes	No	Yes	No	Yes

VI. CONCLUSION

A 4^{th} order RF ΣΔ ADC clocked at 3.6GHz and centered at 900MHz was presented. The ΣΔ ADC architecture is composed of 2 LC tank circuits with Q-enhancement, 3 transconductors, 1 single-bit comparator and 3 single-bit NRZ feedback DACs. In order to tune and calibrate the ΣΔ loop filter, a simple algorithm, suitable for integration, was presented. The ADC was implemented in a standard 130nm CMOS technology and achieved a 52dB SFDR and a 50dB SNDR in a 28MHz BW with only 15mW power consumption. Due to the simplicity of its architecture, the FoM of the ADC is as low as 1pJ/bit, which is to date the best reported RF ΣΔ ADC.

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