Simple architecture for subsampling LC-based ΣΔ modulators

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A simple architecture for subsampling LC-based continuous-time ΣΔ modulators is introduced. The concept of utilising loop delay to simplify the modulator architecture is generalised to subsampling modulators. Moreover, it is shown that is possible to remove the delay-compensation branch usually used in traditional designs. Removing the delay-compensation branch results in significant simplification of the modulator architecture, and eliminates several problems usually associated with the delay-compensation branch.

Introduction: RF continuous-time (CT) ΣΔ modulators provide a promising solution for realising RF analogue-to-digital converters (ADCs) that are capable of direct digitisation of RF signals, and moving most of the signal processing to the flexible and programmable digital domain [1]. LC filters are the best candidates for such RF modulators, owing to their higher speed and dynamic range, compared to Gm-C and RC filters [2]. However, for LC-based modulators, the number of available nodes for feed-forward or feedback coefficients is half the modulator order, which is not sufficient to implement the desired noise transfer function (NTF) [3].

Additional degrees of freedom can be added by using multi-feedback DAC architectures as in [2, 4]. However, this approach suffers from increased complexity of the DAC circuitry which is usually accompanied by increased power consumption and thermal noise power.

A simple architecture for LC-based modulators was proposed in [5], where the loop delay was utilised to reduce the number of feedback DAC branches to only three, as shown in Fig. 1. The first branch is the main DAC, which is connected to the input node. The second branch is the internal DAC, which is connected to the internal node. The third branch is the delay-compensation DAC, which is connected directly before the comparator.

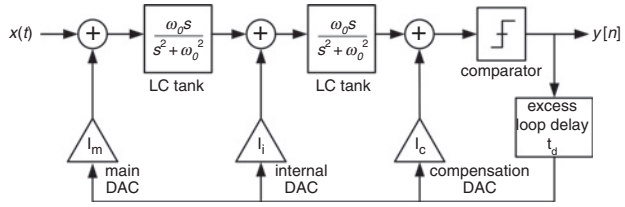

Fig. 1 *Architecture proposed in [5]*

In this Letter, the concept of utilising loop delay to simplify LC-based modulator architecture is generalised to subsampling modulators. The proposed architecture is even much simpler than the original one presented in [5], as it uses only two feedback branches instead of three. The proposed architecture also eliminates the need for the delay-compensation branch which is difficult to implement in high-speed modulators.

Subsampling modulator: In bandpass CT ΣΔ modulators, the sampling frequency f_s is usually four times the centre frequency of the input signal f_o to simplify the design of the preceding downconversion mixer [2]. However, in RF modulators where the centre frequency is very high, the required sampling frequency becomes very high and not suitable for available CMOS processes. Subsampling can be used to reduce the sampling frequency to relax the comparator requirements and reduce power consumption [1, 6].

The architecture proposed in [5], which is shown in Fig. 1, can be extended to the subsampling modulator. To find the range of loop delay for which the modulator is stable, the DAC coefficients are calculated for each value of loop delay. Then, the modulator is simulated and the maximum achievable SNR measured [5]. The DAC coefficients against loop delay and the corresponding SNR are shown in Figs. 2 and 3, respectively. It can be deduced from Fig. 3 that the subsampling modulator can achieve an acceptable SNR over two ranges of loop delay. The first range of normalised loop delay is from 0 to 0.2, which is too small for practical implementation. The second range is from 0.6 to 0.85, which is suitable for implementation. This means that it is possible to design the subsampling modulator using the approach proposed in [5] with three feedback coefficients. However, the subsampling has an additional interesting property. As can be seen in Fig. 2, the value of delay-compensation DAC reaches zero when the normalised loop delay is approximately 0.65. This suggests that if the loop delay is kept close to this value, the compensation DAC branch can be removed. To validate this conclusion, the subsampling modulator was redesigned without the compensation DAC branch, as shown in Fig. 4. The DAC coefficients were then calculated for each value of loop delay, and the modulator SNR was extracted from simulation, as shown in Fig. 5. It can be concluded from the Figure that an acceptable SNR can be obtained over a reasonable range of loop delay. The range of usable loop delay is less wide compared to the first case, because the degrees of freedom is reduced in this case. However, the required range of the loop delay is still feasible to obtain with normal process variations.

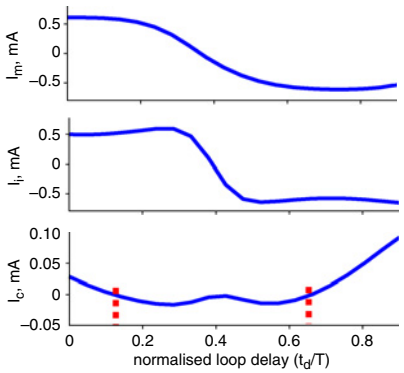

Fig. 2 *DAC coefficients against loop delay in subsampling modulator*

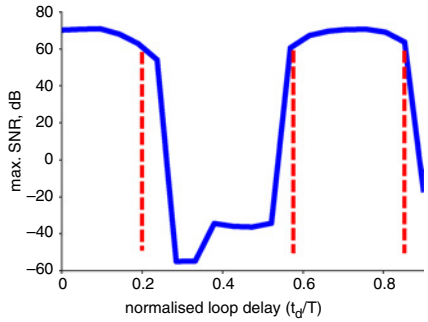

Fig. 3 *SNR against loop delay in subsampling modulator*

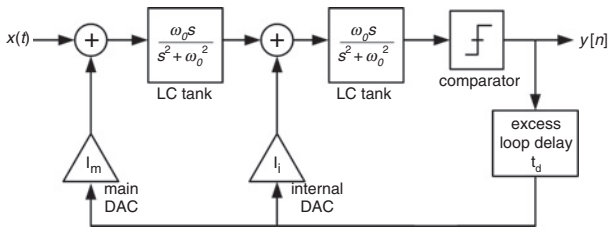

Fig. 4 *Proposed architecture for subsampling modulator*

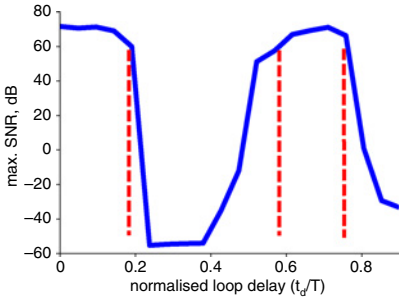

Fig. 5 *SNR against loop delay in subsampling modulator without compensation branch*

Conclusion: The simplified modulator architecture for LC-based CT ΣΔ modulators that was presented previously has been generalised to subsampling modulators. The subsampling modulator shows an additional interesting property that makes it possible to remove the delay-compensation branch and limit the feedback branches to only two branches. This simplifies the modulator circuit and eliminates the problems associated with the summing node needed for delay-compensation DAC.

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One or more of the Figures in this Letter are available in colour online.

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