Sine-Shaping Mixer for Continuous-Time ΣΔ ADCs

Ahmed Ashry and Hassan Aboushady
LIP6 Laboratory, University of Pierre & Marie Curie, Paris VI, France.
Email: ahmed.ashry@lip6.fr

***Abstract*— Sine-shaping of feedback DAC current in continuous-time ΣΔ ADCs is an effective solution to enhance their immunity to clock jitter. In this paper, a simple mixer circuit for producing a sine-shaped output in continuous-time ΣΔ ADCs is introduced. The proposed solution does not need extra clock source or synchronization circuit, as the mixer utilizes the same clock applied to the comparator. It is also shown the that the proposed circuit is immune to temperature and process variations. Simulation results of the proposed circuit implemented in 130nm CMOS process show good agreement with the expected results.**

I. Introduction

Continuous-Time (CT) ΣΔ Analog-to-Digital Converters (ADCs) are receiving more and more attention due to their advantages compared to Discrete-Time (DT) ΣΔ ADCs. Inherent anti-aliasing filtering, lower thermal noise, higher sampling rate and lower power consumption are all attractive advantages of CT ΣΔ ADCs that make them interesting solutions for high data-rate wireless communication systems . Bandpass CT ΣΔ ADCs are considered a promising technique for realizing software defined radio (SDR), as they can achieve a reasonable dynamic range by converting only the band of interest around the desired center frequency. Thus, the direct digitization of the RF signal is possible and almost all the signal processing can be done in the flexible and programmable digital domain [1].

The main disadvantage of CT ΣΔ ADCs is their sensitivity to the clock jitter of the feedback Digital-to-Analog Converter (DAC). The clock jitter noise of the feedback DAC is not shaped by the loop filter, due to its direct connection to the input node, as shown in Fig. 1. It appears as a white noise in the signal band, and causes a degradation in the Signal-to-Noise-Ratio (SNR) of the ADC [2].

The feedback DAC output waveform can be shaped to reduce the jitter effect by using a sine shaped (Sine) DAC as in [3]–[5], or by using a Switched-Capacitor (SC) DAC as in [6], [7]. However, it was shown in [8] that SC DAC is not suitable for bandpass or RF ADCs due to its highpass shaping of clock jitter noise. The comparison of the jitter performance between the different types of feedback DACs in bandpass ΣΔ ADCs done in [8] concluded that Sine DAC is the best, as shown in Fig. 2.

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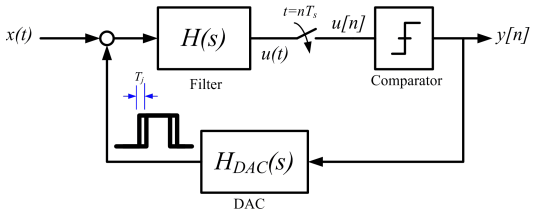


Fig. 1. Continuous-time ΣΔ ADC.

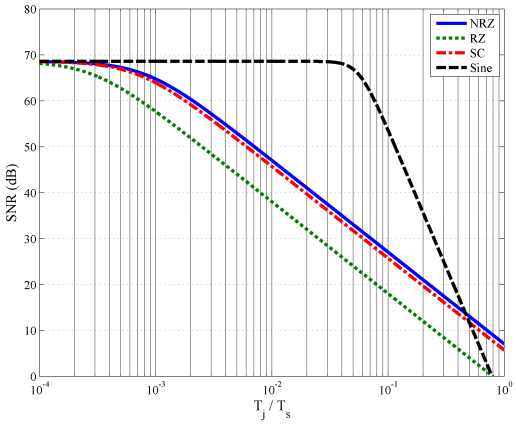
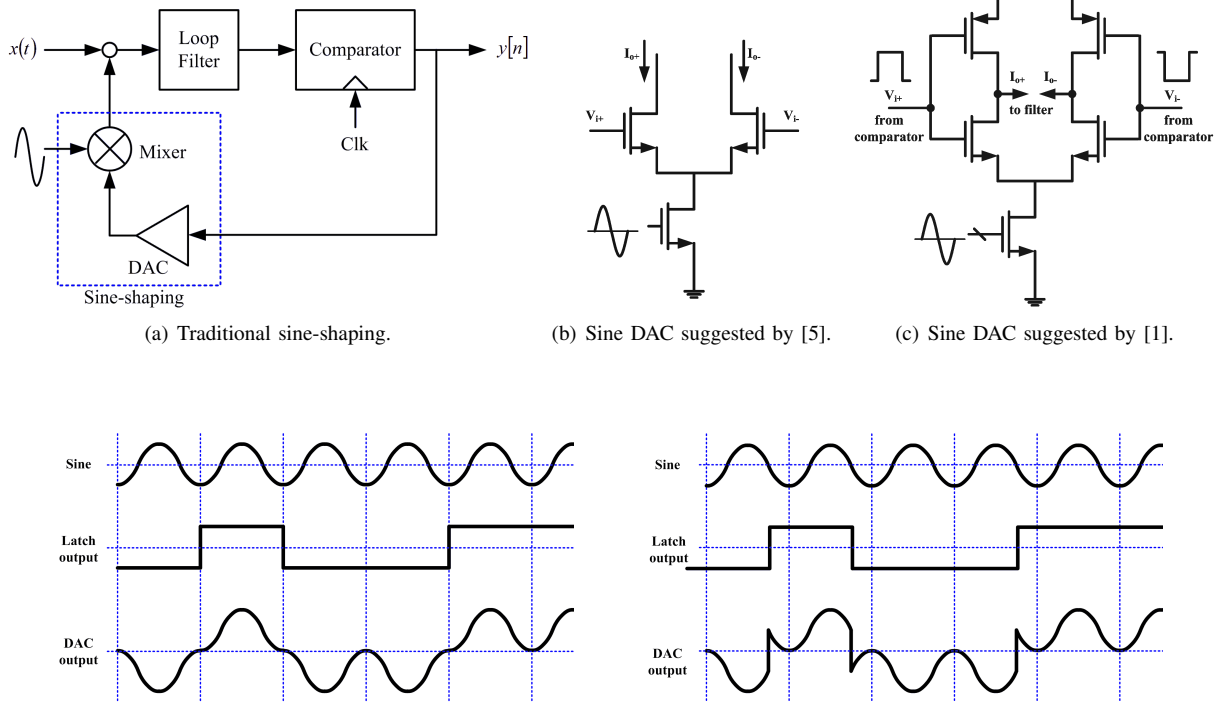


Fig. 2. SNR versus clock jitter of a $4th$ order bandpass CT ADC with OSR=64 for different types of feedback DACs [8].

Another reason for using Sine DAC in RF ΣΔ ADCs is its convenience for sub-sampling technique. This technique, which sometimes called "undersampling" as in [4] or "mirrored-image" as in [9], can reduce the required sampling frequency significantly [10], but it has some issues. One of the main issues is that the ADC output frequency is different from its center frequency. Consequently, the feedback DAC has to give sufficient amplification to the image of the ADC output which coincides with the center frequency. Sine DAC has this property [4].

Although the concept of using sine-shaped DAC is clear, there is no efficient circuit proposed to do the sine-shaping. The authors in [4], [5] suggested to add a sine-shaped tail current to the DAC circuit, but they did not mention how to guarantee the synchronization between tail current and DAC input.

In this work, we propose a simple sine-shaping mixer circuit that does not need extra sine-wave source, as it utilizes the



(a) Traditional sine-shaping. (b) Sine DAC suggested by [5]. (c) Sine DAC suggested by [1].

(d) Ideal sine DAC waveforms. (e) Distorted DAC output due to clock phase shift error.

Fig. 3. Traditional sine-shaping concept, circuits and problems.

same clock applied to the comparator circuit. The proposed circuit eliminates the need for synchronization between different sources and guarantees stable performance across process corners.

The paper is organized as follows: Section II reviews the traditional methods for sine shaping and discusses the previously published techniques. Section III presents the proposed architecture and its circuit implementation. Finally, section IV shows some simulation results for the implemented sine-shaping circuit.

II. Traditional Sine-Shaping

Traditional method for sine-shaping is to inject a sinusoidal signal into the DAC and do the mixing within the DAC itself, as shown in Fig. 3(a). Fig. 3(b) shows the circuit implementation of the Sine DAC suggested by [5], where the DC tail current of the DAC is replaced with a sine-shaped one. The circuit used in [1] is based on the same concept, but it contains additional PMOS DAC that reuses the current of the NMOS DAC, as shown in Fig. 3(c).

Ideally, the sinusoidal signal injected into the DAC should be synchronized with the output bit-stream from the comparator, such that to make the transitions of the bit-stream coincide with the minima of the sine-shaped tail current. If the synchronization is accurate, the Sine DAC will produce a clean output like the one shown in Fig. 3(d).

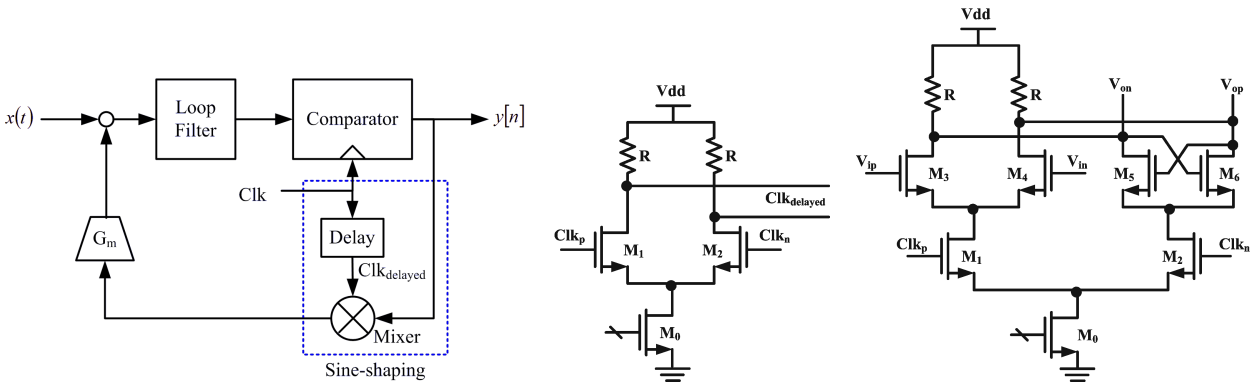
However, it is difficult to achieve perfect phase synchronization between the sine-shaped tail current and the bit-stream, because it requires an accurate estimation and control of many parameters. The phase mismatch between the tail current and the bit-stream leads to a distorted DAC output, as shown in Fig. 3(e). This distorted DAC output degrades the jitter immunity and can even cause a complete failure of the $\Sigma\Delta$ ADC.

III. Proposed Sine-Shaping

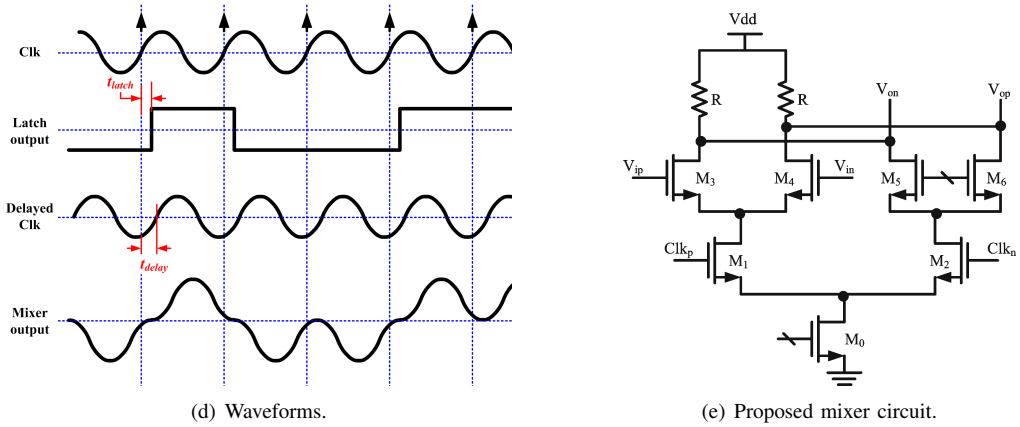
A. Architecture

The proposed architecture is based on doing the sine-shaping directly after the comparator by adding a mixer, as shown in Fig. 4(a). The mixer is driven with the same clock source applied to the comparator, to guarantee the synchronization between the bit-stream and the mixing sinusoidal ($CLK_{delayed}$) . It may appear strange to use a sinusoidal signal as a clock to the comparator, but this is usually the case in high-speed ADCs that work at several GHz sampling frequency.

The delay element needed to adjust the phase of the mixing sinusoidal ($CLK_{delayed}$), can be a simple differential-pair buffer as shown in Fig. 4(b). The delay element circuit is designed mainly to achieve a certain delay (t_{delay}), to produce a clean sine-shaped output, as shown in Fig. 4(d). However,



(a) Proposed sine-shaping technique. (b) Delay element circuit. (c) Latch circuit.



(d) Waveforms. (e) Proposed mixer circuit.

Fig. 4. Proposed sine-shaping technique.

the delay element can add more value to the proposed sine-shaping architecture. If the latch (used inside the comparator and shown in Fig. 4(c)) and the delay element are using a similar circuit topology and the same type of load resistors and transistors, the latch delay (t_{latch}) and t_{delay} will track each other. This makes the overall performance more immune to process and temperature variations.

B. Proposed Mixer Circuit

The mixer needed to do the sine-shaping is quite different from traditional mixer. The traditional mixer multiplies the input by a sinusoidal, while the needed mixer should multiply the input by a DC-shifted sinusoidal "raised cosine" to produce the needed sine-shaped output.

The proposed mixer circuit shown in Fig. 4(e) is a modified version of popular double-balanced Gilbert cell. The modification is that the switching transistors in the right section "M_5 and M_6" are connected to a DC bias instead of being connected to the mixer input. With this modification, the right section does not contribute to the differential output current. The left section, which can be seen as a single-balanced mixer, is the only source of differential output current and is given by:

$$I_{diff} = I_{dc}\,(1 + sin\,(2\pi f_s t))\;V_i(t) \tag{1}$$

where I_{dc} is the DC tail current, f_s is the sampling frequency and $V_i(t)$ is the mixer input.

The common-mode output current due to the left section is given by:

$$I_{cm,left} = 0.5\,I_{dc}\,(1 + sin\,(2\pi f_s t)) \tag{2}$$

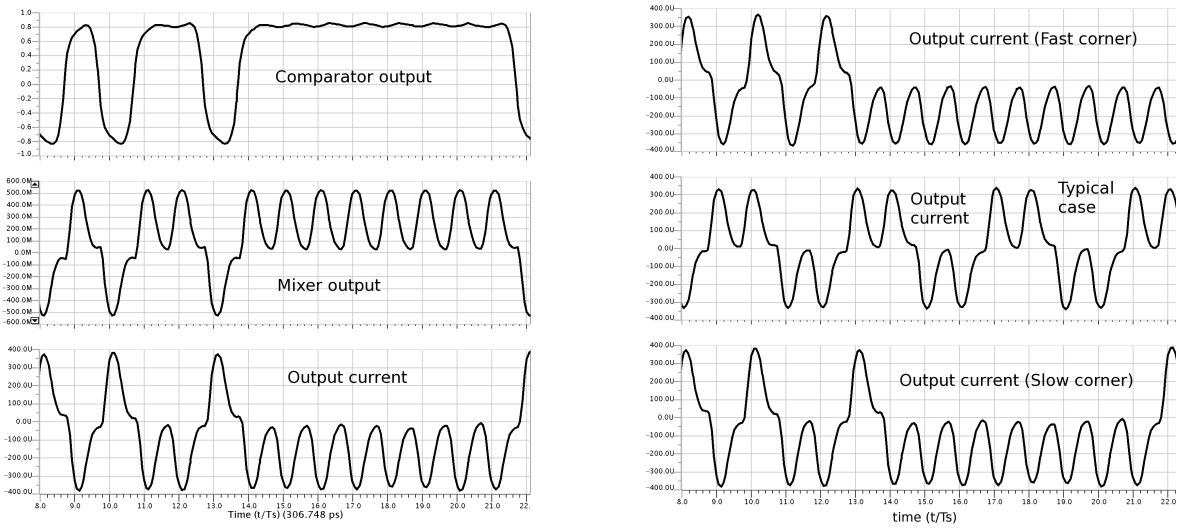
And the common-mode output current due to the right section is given by:

$$I_{cm,right} = 0.5\,I_{dc}\,(1 - sin\,(2\pi f_s t)) \tag{3}$$

By combining 2 and 3, the common-mode output current is found to be equal to I_{dc}. This means that the output common-mode is DC and there are no common-mode time-variance, which simplifies the design of the preceding DAC circuit and prevent any possible common-mode instabilities.

IV. Simulation Results

The proposed sine-shaping architecture and mixer circuits was used to implement a subsampling 4^{th} order LC-based $\Sigma\Delta$ ADC centered at 2.45GHz and sampled at 3.26GHz in 130nm CMOS process. Fig. 5(a) shows the simulation results of the proposed mixer circuit, which shows a good agreement with the expected results.



(a) Simulation results.

(b) Corners.

Fig. 5. Simulation results of proposed sine-shaping mixer

To investigate the effect of process variations, the designed ADC was simulated at two extreme corners. Fig. 5(b) shows the simulated DAC output current in the three cases: the slow corner (SS), the typical case (TT) and the fast corner (FF). It can be seen that the DAC has a clean sine-shaped output current in the three cases, which assures that the proposed sine-shaping architecture is immune to process variations.

V. Conclusion

A simple and rigid architecture for producing a sine-shaped feedback DAC current in continuous-time $\Sigma\Delta$ ADCs was proposed. The proposed architecture includes a modified mixer circuit that produces a clean sine-shaped output with a constant DC common-mode output. The proposed solution does not need extra clock source or synchronization circuit, as the mixer uses the same clock applied to the comparator. With proper design the proposed architecture can be made immune to temperature and process variations and achieve the optimum performance expected from the ADC.

References

[1] N. Beilleau, H. Aboushady, F. Montaudon, and A. Cathelin, "A 1.3V 26mW 3.2Gs/s undersampled LC bandpass $\Sigma\Delta$ ADC for a SDR ISM-band receiver in 130nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium, (RFIC'09)*, June 2009, pp. 383–386.

[2] J. Cherry and W. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 6, pp. 661–676, June 1999.

[3] A. Pulincherry, M. Hufford, E. Naviasky, and U.-K. Moon, "A time-delay jitter-insensitive continuous-time bandpass $\Delta\Sigma$ modulator architecture," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 10, pp. 680–684, Oct. 2005.

[4] N. Beilleau, C. Ouffoue, and H. Aboushady, "Sinusoidal RF DACs for undersampled LC bandpass $\Sigma\Delta$ modulators," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS'07)*, Aug. 2007, pp. 1477–1480.

[5] S. Luschas and H. Lee, "High-speed $\Sigma\Delta$ modulators with reduced timing jitter sensitivity," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 11, pp. 712–720, Nov. 2002.

[6] F. Gerfers, M. Ortmanns, and Y. Manoli, "Design issues and performance limitations of a clock jitter insensitive multibit DAC architecture for high-performance low-power CT $\Sigma\Delta$ modulators," in *Proc. IEEE International Symposium on Circuits and Systems, (ISCAS'04)*, vol. 1, May 2004, pp. 1076–1079.

[7] R. Veldhoven, "A triple-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2069–2076, Dec. 2003.

[8] A. Ashry and H. Aboushady, "Jitter analysis of bandpass continuous-time $\Sigma\Delta$Ms for different feedback DAC shapes," in *Proc. IEEE International Symposium on Circuits and Systems, (ISCAS'10)*, May 2010, pp. 3997–4000.

[9] J. Ryckaert, J. Borremans, B. Verbruggen, L. Bos, C. Armiento, J. Craninckx, and G. Van der Plas, "A 2.4 GHz low-power sixth-order RF bandpass $\Delta\Sigma$ converter in CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2873–2880, Nov. 2009.

[10] A. Ashry and H. Aboushady, "Simple architecture for subsampling LC-based $\Sigma\Delta$ modulators," *Electronics Letters*, vol. 46, no. 18, pp. 1263–1264, Sept. 2010.