Scaling Input Signal Swings of Overloaded Integrators in Resonator-based Sigma-Delta Modulators

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***Abstract*—Overloading of the integrators in loop filter of Sigma-Delta modulators is a performance degrading factor in circuit implementations. In this paper, it is shown that in resonator-based ΣΔ modulators scaling factors should be introduced in order to adjust the integrators' input. A systematic method is presented to calculate these scaling factors without modifying the noise and signal transfer functions. The effect of the scaling factors on circuit implementation is also discussed. Several examples are given to illustrate the influence of the scaling factors on the ΣΔ performances depending on the order, architecture and number of bits of the quantizer.**

I. INTRODUCTION

Sigma Delta ADCs are very popular due to their high resolution capability with more relaxed analog component specifications. Many works have been published on discrete-time (DT) and continuous-time (CT) design methodologies at the system level [1][2]. Clearly, for circuit level implementations, all the signal swings resulting from the system level design must be within allowed limits. The problem on limiting output signal swings of the integrators of ΣΔ Modulator was studied in [3], but large input signal swings of the integrators are also problematic. Input signal swings must be scaled down to allowable limits so that the integrators stay in their normal operating region and no related performance losses occur in the modulator.

In this paper, we present a simple method for limiting the input signal swings of the integrators in ΣΔ modulators suitable for both DT and CT architectures with feedforward (FF), Fig. 1, and feedback (FB), Fig. 2, loop filter topologies. It will be shown that the method does not change the Signal and Noise Transfer Functions, (STF and NTF), of the modulator and significantly improves the SNR degraded due to overloading of integrators in the system level. In section II, we explain the method and present a simple approach for finding the scaling factors. Possible non-idealities arising from circuit level implementation issues are discussed in section III.

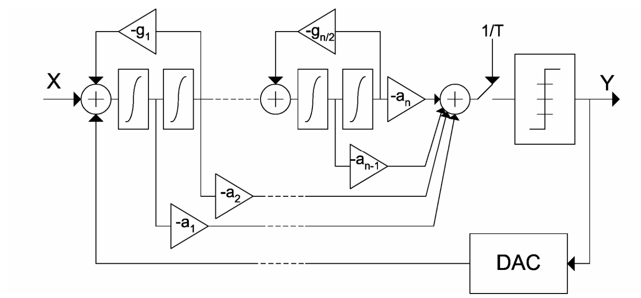

Figure 1. Feedforward architectures of Sigma-Delta Modulators (CRFF)

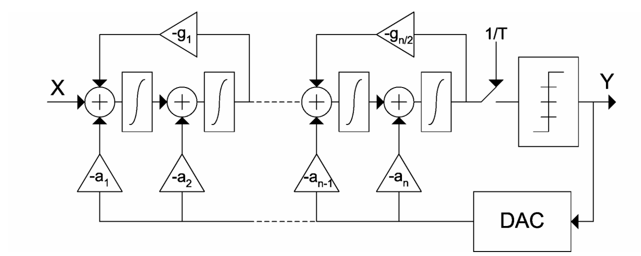

Figure 2. Feedback architectures of Sigma-Delta Modulators (CRFB)

Various examples showing the effectiveness of the method are given in section IV. And the paper is concluded in section V.

II. DESCRIPTION OF THE SCALING METHOD

In even order architectures, because of the feedback coefficient of the resonator, the most critical signal swings occur at inputs of the first (front) integrators of the resonators in the loop filter. So, although the method is general (i.e. can be applied for limiting any integrator's input signal swing in both FF and FB topologies), it is useful mainly for limiting the critical input signal swings of the first integrator in resonators of the loop filter. In the following, we'll explain the method by focusing on a resonator structure.

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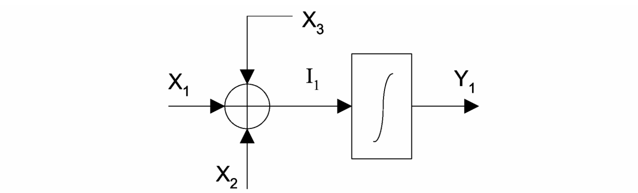

Figure 3. General structure for the application of $1/k_i$ scaling method

A. $1/k_i$ Scaling Method

Fig. 3. shows the general form of the front part of a resonator, which is a common structure in both even-order FF and FB topologies.

The method can be described with the help of Fig 3. shortly as follows: the input signals to the summer unit are linearly scaled down by division with a 'k_i' factor (resulting in a reduced signal swing at the input of the integrator), and then the output signal of the integrator is scaled up by multiplication with the same 'k_i' factor. Fig. 4. illustrates the $1/k_i$ scaling method graphically.

B. Conservation of Transfer Funtions

The method can easily be proved mathematically as follows:

Before $1/k_i$ scaling, (*bs*), (Fig.3) :

$$I_{1,bs} = (X_1 + X_2 + X_3)$$
$$Y_{1,bs} = \int (I_{1,bs})\, dt$$

After $1/k_i$ scaling, (*as*), (Fig. 4) :

$$I_{1,as} = (X_1 + X_2 + X_3)\,\frac{1}{k_i} = I_{1,bs}\,\frac{1}{k_i}$$
$$Y_{1,as} = k_i \int \left(I_{1,bs}\,\frac{1}{k_i}\right) dt = k_i \left(\int I_{1,bs}\, dt\right) \frac{1}{k_i}$$
$$Y_{1,as} = Y_{1,bs}$$

(Although the proof is given for CT case, equations are also the same for the DT case).

It is clear from the above calculations that, while we get a scaled signal, (I_1/k_i), at the input of the integrator, the output signal, (Y_1), remains unchanged which means that the input-output relation does not change with the addition of k_i factors. So, the method preserves all the transfer functions of modulator and is valid for both FF and FB topologies as it is for DT and CT cases.

C. Determination of $1/k_i$ Scaling Factors:

Since ΣΔ modulators are non-linear systems because of the quantizer inside, practically we use behavioral simulations [3] [4] [5] for determining the $1/k_i$ coefficients.

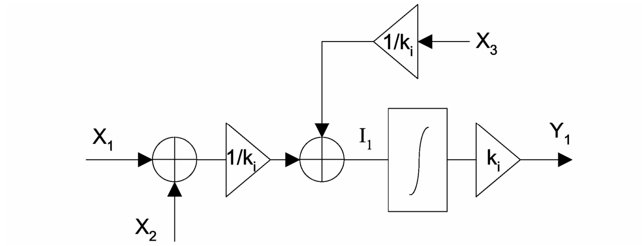

Figure 4. General structure after the application of $1/k_i$ scaling method

Using an ideal model with an input signal of sine wave with frequency in bandwidth and peak-SNR amplitude, k_i factors for each of the integrators (most often, the first integrators of resonators) in the loop filter may be determined one by one. But, since the method preserves the output signals of integrators (Y1 in Fig.3 and Fig.4), the value of the k_i^{th} factor has no effect on k_{i+1}^{th} factor, and so the order of determination is not important. k_i factors may be determined as follows:

1) Simulate the modulator and determine the "critical" integrators which have input signal swing peak amplitudes larger than the allowed limits (i.e.overloading thresholds).

2) For every critical integrator, using the following formula, calculate the k_i scaling factor.

$$k_i = \frac{\max\,(\text{input swing of the } i_{th} \text{ critical integrator})}{\text{desired (input swing of the } i_{th} \text{ critical integrator)}}$$

Naturally, system and circuit level design choices will specify the levels of maximum allowable input signal swings of the resonators.

III. Circuit Implementation Issues

From the point of view of implementation, it is obvious that k_i factors may easily be realized by joining them with the nearest gain stages. For example the $1/k_i$ factor on the feedback path of a resonator can be absorbed by the gain stage implementing the feedback coefficient. And also the k_i factor after the integrator can be realized by including it within the gain of the integrator. So generally, less than 3 separate $1/k_i$ blocks will be enough for implementing the method.

The most problematic place for this separate $1/k_i$ factor is the one that is placed just in front of the loop filter (after the differencing unit which outputs the error signal of the modulator) for limiting the signal swing of the first integrator (most often the first one within the resonator structure). Since this block is the most critical one, we may call it shortly as $1/k_f$, where 'f' stands for the word 'front'. As it will be the first stage of the loop filter, this $1/k_f$ block's gain and noise performance will have great effect on the overall noise figure (NF) of the loop filter. And since $1/k_i$ factors will always be smaller than 1, this separate $1/k_f$ block will always increase the NF of the loop filter and adversely affect the overall performance of the modulator. But considering the contribution of the $1/k_i$ scaling method to the SNR performance of the modulator (~ 39dB for a 4th order Cascade of Resonators Feedforward (CRFF) type CT bandpass SD Modulator, Fig. 5), the effect of increase in NF of the loop filter becomes unimportant. As a result, it can be said that $1/k_i$ factors must be chosen as high as possible, closer to 1.

IV. DESIGN EXAMPLES

In the examples following, we have used ideal behavioral models of bandpass CT ΣΔ modulators with an oversampling ratio (OSR) of 128 and made SNR calculations with 16384 time points. -6 dBFS (sine wave) was used for the input amplitudes, this is a reasonable common condition for simulations, since all the modulators approach their peak-SNR around -6 dBFS. In the behavioral models, DT coefficients (from R. Schreier toolbox, [5]) transformed into CT coefficients with the techniques given in [2] [3] were used. The simulated models are as following:

a) Mono-bit quantizer : 2, 4 and 6th order with CRFF topology and 4th order with CRFB topology.

b) Multi-bit quantizer (2 and 3 bits) : 4th order with CRFF and 4th order with CRFB topology.

The simulations were done with and without saturation blocks at the inputs and outputs of the integrators. And it was assumed that, as the case for a mono-bit quantizer, the integrators were also overloaded with input amplitudes larger than ± 2 (normalized to 1/Vref).

Fig. 6. shows a histogram plot of the input signal of the first integrator of a 4th order CT bandpass ΣΔ Modulator with CRFF topology. The modulator model does not include saturation blocks at the inputs and outputs of the integrators. Assuming the normal operating region for this integrator is ± 2 (normalized to 1/Vref), it is clear that this integrator will be overloaded and cause a degradation in SNR of the modulator. In Fig 7., we see the limiting effect of using $1/k_i$ scaling method (with k_1=2), on the histogram plot of the same signal with same conditions.

Fig. 5. shows the DR plots of the mono-bit 4th order CT bandpass ΣΔ modulator with CRFF topology for three cases: the first one for the ideal case representing no overloading of integrators (without saturation blocks at the inputs and outputs of the integrators), the second one for the case of overloading of integrators (with saturation blocks at the inputs and outputs of the integrators), and the third one for the case of application of $1/k_i$ scaling method in saturation conditions. It is clear from the figure that, the method greatly restores the SNR (heavily degraded due to saturation conditions), back to the one in ideal case of no overloading of integrators.

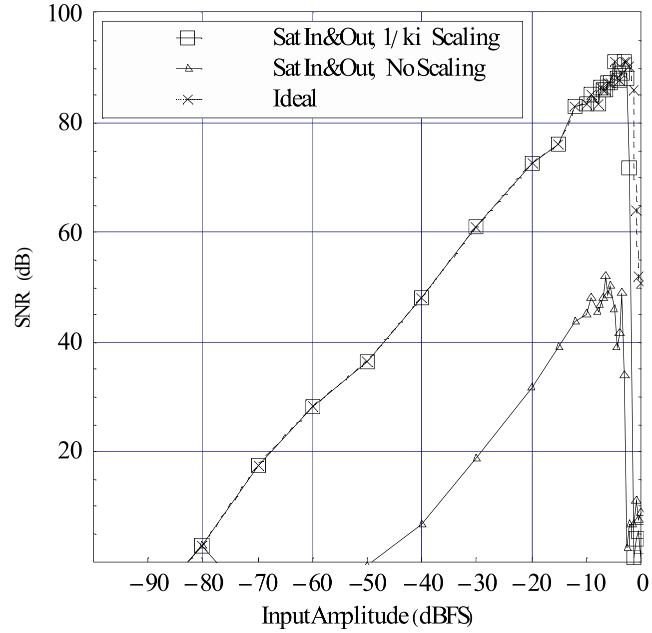

Figure 5. SNR plot of 1-bit 4th Order CT Bandpass ΣΔ CRFF Topology illustrating the effectiveness of the method

In Table I., we see the effect of the method on the SNR performance of mono-bit modulators with different orders of loop filter all with CRFF topology. The important point in Table I. is that k_l factors are very close to each other (~ 1.65, scaling the signal swings to 1.9) for different orders. They form the $1/k_f$ factors in front of the loop filter, and nearly do not change with the order.

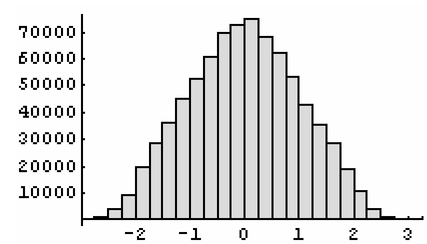

Figure 6. Histogram plot illustrating the signal swing at the input of the first integrator in 1-bit 4th order CRFF topology before $1/k_i$ scaling

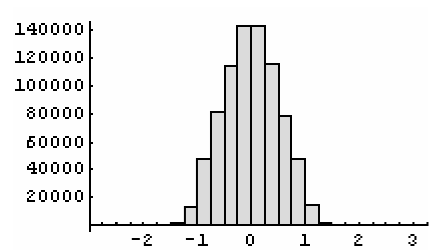

Figure 7. Histogram plot illustrating the signal swing at the input of the first integrator in 1-bit 4th order CRFF topology after $1/k_i$ scaling

TABLE 1. SIMULATION RESULTS OF MONO-BIT BANDPASS CRFF MODULATORS WITH DIFFERENT ORDERS

Mono-bit	CRFF 2	CRFF 4	CRFF 6
SNR (Ideal) No Saturation Blocks ***No 1/k_i Scaling***	61.339	87.144	100.514
SNR Sat Blocks In & Out ***No 1/k_i Scaling***	38.122	48.365	Unstable
Int1_In_Max	3.0632	2.99	3.1653
Int3_In_Max	-	1.8327	1.1977
Int5_In_Max	-	-	4.6724
k1	1.6122	1.5736	1.6659
k2	-	0.9645	0.6303
k3	-	-	2.4591
SNR Sat Blocks In & Out ***With 1/k_i Scaling***	61.339	87.144	100.514

We see the effect of the method on multi-bit cases in Tables 2 and 3. As the number of bits of the quantizer (N) increases, the peak amplitudes of signal swings at the inputs of integrators decrease in general, meaning that value of k_i factors also decrease, which is good for the NF of the loop filter. For example k_i factors become useless for the CRFF topology of 4^{th} order with N=3.

TABLE 2. SIMULATION RESULTS OF CT 4TH ORDER BANDPASS CRFF MODULATORS WITH MONO-BIT AND MULTI-BIT QUANTIZERS

CRFF 4th Order	1-Bit	2-Bit	3-Bit
SNR (Ideal) No Saturation Blocks ***No 1/k_i Scaling***	87.144	92.886	98.894
SNR Sat Blocks In & Out ***No 1/k_i Scaling***	48.365	91.594	98.894 (No need for scaling)
k1	1.5736	0.6971	0.5320
k2	0.9645	1.0853	0.6094
SNR Sat Blocks In & Out ***With 1/k_i Scaling***	87.144	92.886	98.894 (Without scaling)

TABLE 3. SIMULATION RESULTS OF CT 4TH ORDER BANDPASS CRFB MODULATORS WITH MULTI-BIT QUANTIZERS

CRFB 4th Order	1-Bit	2-Bit	3-Bit
SNR (Ideal) No Saturation Blocks ***No 1/k_i Scaling***	87.040	95.038	97.016
SNR Sat Blocks In & Out ***No 1/k_i Scaling***	37.341	unstable	63.608
k1	1.9978	1.5638	1.4295
k2	1.6282	0.6896	0.5885
SNR Sat Blocks In & Out ***With 1/k_i Scaling***	87.743	95.038	97.016

Observing Table 2. (CRFF 4^{th} Order) and Table 3. (CRFB 4^{th} Order), we see that integrators in the FB topologies suffer more from the overloading of integrators compared to FF topologies, consistent with the idea that, mainly, the feedback coefficients (especially the large ones) cause overloading of the front integrators in resonators of the loop filter.

V. CONCLUSION

In this paper, we have presented a scaling method for limiting the input signal swings of integrators, which is valid for FF and FB topologies of DT and CT ΣΔ Modulators. The method greatly improves the performance of modulators suffering from SNR degradation due integrators' input overload. Several examples were given to demonstrate the effectiveness of the proposed method. It has been shown that the scaling method is particularly important in mono-bit as well as feedback architectures.

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