A Generalized Approach to Design CT $\Sigma\Delta$ Ms based on FIR DAC

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Abstract— In this paper, a generic and simple approach to design Continuous-Time Sigma-Delta Modulators (CT $\Sigma\Delta Ms$) based on Finite Impulse Response Digital-to-Analog Converter (FIR DAC) is introduced. The numerical conversion from Continuous-Time to Discrete-Time allows the designer to explore complex modulator architectures and different feedback DAC shapes, without dealing with difficult equations needed in other published design approaches.

I. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators ($\Sigma\Delta Ms$) are receiving more and more attention due to their advantages compared to Discrete-Time (DT) $\Sigma\Delta Ms$. Inherent antialiasing filtering, lower thermal noise, higher sampling rate and lower power consumption are all attractive advantages of CT $\Sigma\Delta Ms$ that make them interesting solutions for high datarate wireless communication systems [1].

On the other hand, the mixed-signal nature of CT $\Sigma\Delta Ms$ makes their design and analysis more complicated than its DT counterpart. An efficient way to design a CT $\Sigma\Delta M$ is to start by calculating its DT equivalent model, as shown in Fig. 1, by converting the loop gain from s-domain to z-domain using the impulse invariant transformation [2]:

$$G_{CT}(z) = Z \left\{ L^{-1} [H(s) H_{DAC}(s)]_{t=nT_s} \right\}$$
(1)

where H(s) is the transfer function of the loop filter, $H_{DAC}(s)$ is the feedback Digital-to-Analog Converter (DAC) transfer function and T_s is the sampling time. This z-domain loop gain can be calculated numerically using Matlab® CT-to-DT conversion function "c2d", and it has the general form:

$$G_{CT}(z) = \frac{B_{CT}(z)}{A_{CT}(z)} = \frac{b_{CT0} + b_{CT1}z^{-1} + \dots + b_{CTk}z^{-k}}{a_{CT0} + a_{CT1}z^{-1} + \dots + a_{CTn}z^{-n}}$$
(2)

Usually this loop gain, which will be referred as CT LG, is not optimal and needs to be modified to match the optimal loop gain of the DT $\Sigma\Delta M$ of the same type and order, which is calculated using Schreier toolbox [3]. This optimal discrete time loop gain will be referred as DT LG, and it has the general form:

$$G_{DT}(z) = \frac{B_{DT}(z)}{A_{DT}(z)} = \frac{b_{DT0} + b_{DT1}z^{-1} + \dots + b_{DTn}z^{-n}}{a_{DT0} + a_{DT1}z^{-1} + \dots + a_{DTn}z^{-n}}$$
(3)



Figure 1. Equivalence between CT and DT $\Sigma\Delta Ms$.

There are several techniques to match CT LG to DT LG. The direct method is to design the CT filter coefficient to match the DT equivalent as in [4]. This method is simple, but it is not suitable for LC based modulators, where there are no sufficient degrees of freedom to change the filter coefficients. Another technique is to use multi-feedback by adding a delayed version of the feedback DAC [5] or an integrating feedback DAC [6]. The multi-feedback technique was generalized by [7] to a more flexible technique based on matching the loop gain using FIR (Finite Impulse Response) DAC. The FIR is added between the modulator output and the feedback DAC, as shown Fig. 2, and the FIR coefficients are chosen such that the CT LG multiplied by the FIR is equal to the desired DT LG:

$$G_{DT}(z) = G_{CT}(z) \cdot F(z) \tag{4}$$

The authors of [7] suggested a systematic design approach that is based on equating the partial fractions of both sides to calculate the FIR coefficients. Although this method is accurate, it is very difficult to generalize, due to the complicated formulas used. The method is getting more complicated when applied to higher orders filters or different shapes of the feedback DAC waveforms. In this work, a numerical approach is proposed to overcome the complexity of the analytical equations needed in the design method suggested in [7].



Figure 2. FIR-based CT $\Sigma \Delta M$.

II. PROPOSED APPROACH

A. Approach Concept

As the denominator of CT LG is, by design, equal to DT LG, we need only to match the numerators of both sides, so (4) can be reduced to:

$$B_{DT}(z) = B_{CT}(z) \cdot F(z) \tag{5}$$

By expanding both sides, we get:

$$(b_{DT0} + \dots + b_{DTn} z^{-n}) = (b_{CT0} + \dots + b_{CTk} z^{-k}) \cdot (f_0 + \dots + f_m z^{-m})$$
(6)

By doing the multiplication, which is actually a convolution, we get the following equations set, which can be written in matrix format as:

$$\begin{bmatrix} b_{DT0} \\ b_{DT1} \\ \vdots \\ b_{DTn} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} b_{CT0} & 0 & 0 & \cdots & 0 \\ b_{CT1} & b_{CT0} & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \cdots & 0 \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ b_{CTk} & b_{CTk-1} & b_{CTk-2} & \cdots & b_{CT0} \\ 0 & b_{CTk} & b_{CTk-1} & \cdots & b_{CT1} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & 0 & 0 & \cdots & b_{CTk} \end{bmatrix} \begin{bmatrix} f_0 \\ f_1 \\ \vdots \\ f_m \end{bmatrix}$$
(7)

or symbolically as:

$$[b_{DT}] = [b_{CT}] \cdot [f]$$
(8)

And finally, the FIR coefficients are calculated directly using matrix division:

$$[f] = [b_{CT}]^{-1} \cdot [b_{DT}] \tag{9}$$

B. Half Period Delay DAC

It can be seen that the suggested method is much simpler and more direct. However, the derived equations are valid only for FIR that is clocked at the sampling frequency, i.e. the delay between any two successive samples is T_s . For more flexibility and lower power consumption, the FIR can work at both the positive and the negative clock edges, i.e. the delay between any two successive samples is $T_s/2$ [7]. To generalize the derived equations for this case without adding more complexity, we can divide the FIR into two parts: even part and odd part, as shown in Fig. 3. For this case, the CT LG is composed of two parts, even part and odd part, where the even part is calculated as:



Figure 3. Half period delay FIR DAC.

$$G_{CT_{ev}}(z) = Z \left\{ L^{-1} \left[H(s) H_{DAC}(s) \right]_{t=nT_s} \right\}$$
(10)

and the odd part is calculated as:

$$G_{CT_{od}}(z) = Z \left\{ L^{-1} \left[H(s) H_{DAC}(s) \cdot e^{-s\frac{T_s}{2}} \right]_{t=nT_s} \right\}$$
(11)

Numerically, we can find both parts of CT LG:

$$G_{CT_{ov}}(z) = \frac{B_{CT_{ov}}(z)}{A_{CT}(z)} = \frac{b_{CT_{ov}0} + b_{CT_{ov}1}z^{-1} + \dots + b_{CT_{ov}k}z^{-k}}{a_{CT0} + a_{CT1}z^{-1} + \dots + a_{CT_{n}}z^{-n}}$$
(12)

and

$$G_{CT_{od}}(z) = \frac{B_{CT_{od}}(z)}{A_{CT}(z)} = \frac{b_{CT_{od}0} + b_{CT_{od}1}z^{-1} + \dots + b_{CT_{od}k}z^{-k}}{a_{CT0} + a_{CT1}z^{-1} + \dots + a_{CT_{n}}z^{-n}}$$
(13)

As in the previous case, we need to match CT LG to DT LG:

$$G_{DT}(z) = G_{CT_{ev}}(z) \cdot F_{ev}(z) + G_{CT_{od}}(z) \cdot F_{od}(z)$$
(14)

Again, the denominator is the same, and we need only to match the numerators:

$$B_{DT}(z) = B_{CT_{ev}}(z) \cdot F_{ev}(z) + B_{CT_{od}}(z) \cdot F_{od}(z)$$
(15)

By expansion we get:

By multiplication and writing in matrix format:

$$\begin{bmatrix} b_{DT0} \\ b_{DT1} \\ \vdots \\ b_{DTn} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} b_{CT_{o}0} & 0 & \cdots & 0 & b_{CT_{od}0} & 0 & \cdots & 0 \\ b_{CT_{o}1} & b_{CT_{o}0} & \cdots & 0 & b_{CT_{od}1} & b_{CT_{od}0} & \cdots & 0 \\ \vdots \\ \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ b_{CT_{o}k} & b_{CT_{o}k-1} & \cdots & b_{CT_{o}0} & b_{CT_{od}k-1} & \cdots & b_{CT_{od}0} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \cdots & \vdots \\ 0 & b_{CT_{o}k} & \cdots & b_{CT_{o}1} & 0 & b_{CT_{od}k} & \cdots & b_{CT_{od}1} \\ \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \cdots \\ 0 & 0 & \cdots & b_{CT_{o}k} & 0 & 0 & \cdots & b_{CT_{od}k} \\ \end{bmatrix} \begin{bmatrix} f_{ev0} \\ f_{ev1} \\ \vdots \\ f_{evm} \\ f_{od0} \\ f_{od1} \\ \vdots \\ f_{odm} \end{bmatrix}$$

Finally, the FIR coefficients can be found directly by matrix division.

C. Compensation DAC

In some cases, and due to excess loop delay, the feedback FIR DAC is not sufficient to match CT LG to DT LG. It was proposed in [8] to solve this problem by adding a delay compensation branch as shown in Fig. 4. The loop gain of the compensation branch can be calculated using the same CT-to-DT conversion technique, but due to the fact that the feedback DAC of the compensation branch is connected directly before the sampler, the CT-to-DT conversion is much simpler:

$$G_{CT_{c}}(z) = Z \left\{ L^{-1} \left[H_{DAC}(s) \right]_{t=nT_{s}} \right\} = z^{-1} d(0)$$
(18)

where d(0) is the feedback DAC output at the instance of sampling. Without loss of generality, the value of d(0) can be set to unity. Now the overall CT LG should be matched to the DT LG:

$$G_{DT}(z) = G_{CT_{ov}}(z) \cdot F_{ev}(z) + G_{CT_{od}}(z) \cdot F_{od}(z) + z^{-1} \cdot F_{c}(z) \quad (19)$$

By multiplying both sides with CT LG denominator $A_{CT}(z)$ we get:

$$B_{DT}(z) = B_{CT_{ov}}(z) \cdot F_{ev}(z) + B_{CT_{od}}(z) \cdot F_{od}(z) + z^{-1}A_{CT}(z) \cdot F_{c}(z)$$
(20)

Similar to the previous two cases, the expansion gives:

$$\begin{pmatrix} b_{DT0} + \dots + b_{DTn} z^{-n} \end{pmatrix} = \begin{pmatrix} b_{CT_{c0}} + \dots + b_{CT_{c}k} z^{-k} \end{pmatrix} \cdot \begin{pmatrix} f_{c0} + \dots + f_{cm} z^{-m} \end{pmatrix} + \begin{pmatrix} b_{CT_{cd0}} + \dots + b_{CT_{cd}k} z^{-k} \end{pmatrix} \cdot \begin{pmatrix} f_{c0} + \dots + f_{cm} z^{-m} \end{pmatrix} + \begin{pmatrix} a_{CT0} z^{-1} + \dots + a_{CTk} z^{-k-1} \end{pmatrix} \cdot \begin{pmatrix} f_{c0} + \dots + f_{cm} z^{-m} \end{pmatrix}$$

$$(21)$$

By multiplication and writing in matrix format:

Finally, the FIR coefficients are found by matrix division, as the previous cases.

III. DESIGN EXAMPLE

To validate the proposed technique, it is used to design a 4^{th} order LC-based bandpass CT $\Sigma\Delta M$. The first step is to design the equivalent DT modulator using Schreier toolbox. By using the synthesis function to design a bandpass NTF centered at quarter the sampling frequency with 1.5 out-of-band gain we get the following DT LG transfer function:

$$G_{DT}(z) = \frac{0.77z^{-2} + 0.56z^{-4}}{1 + 2z^{-2} + z^{-4}}$$
(23)

The next step is to design the CT LC filter shown in Fig. 5, such that CT filter poles are coinciding with DT poles:



Figure 4. Adding delay compensation branch

$$H(s) = G_{mc} \left(\frac{\omega_o \cdot L \cdot s}{s^2 + \omega_o^2}\right)^2$$
(24)

where G_{mc} is the coupling transconductance between the two tank circuits, ω_o is the resonance frequency, and *L* is the inductance. In this example, the center frequency is 915MHz, the inductance is 10nH and the coupling transconductance is 1mA/V. The transfer function of the rectangular NRZ feedback DAC is given by:

$$H_{DAC}(s) = \frac{1}{s} \left(1 - e^{-sT_s} \right)$$
(25)

Substituting from (24) and (25) into (10) and (11), the DT equivalent is calculated using Matlab[®] function "c2d" with "impulse sampling" option. The two parts of the CT LG are found to be:

$$G_{CT_{ev}}(z) = \frac{2.8z^{-1} - 2.8z^{-2} - 2.8z^{-3} + 2.8z^{-4}}{1 + 2z^{-2} + z^{-4}}$$
(26)

$$G_{CT_{od}}(z) = \frac{z^{-1} + 2z^{-2} - 6z^{-3} + 2z^{-4} + z^{-5}}{1 + 2z^{-2} + z^{-4}}$$
(27)

Substituting from (23), (26) and (27) in (22), we get the following set of equations:

$$\begin{bmatrix} 0\\0\\0,77\\0\\0.56\\0\\0\\0\\0\end{bmatrix} = \begin{bmatrix} 0&0&0&0&0&0&0&0&0\\2.8&0&0&1&0&0&1&0&0\\-2.8&2.8&0&2&1&0&0&1&0\\-2.8&-2.8&2.8&-6&2&1&2&0&1\\2.8&-2.8&-2.8&2&-6&2&0&2&0\\0&2.8&-2.8&1&2&-6&1&0&2\\0&0&2.8&0&1&2&0&1&0\\0&0&0&0&0&0&1&0&0&1 \end{bmatrix} \begin{bmatrix} f_{ev0}\\f_{ev1}\\f_{ev2}\\f_{ed0}\\f_{ed1}\\f_{ed2}\\f_{c0}\\f_{c1}\\f_{c2} \end{bmatrix}$$
(28)

By removing the first trivial zeros row of the equations set, and doing matrix division, we get the FIR coefficients:

$$\begin{bmatrix} f_{ev0} \\ f_{ev1} \\ f_{ev2} \end{bmatrix} = \begin{bmatrix} 0.18 \\ 0 \\ 0 \end{bmatrix} \& \begin{bmatrix} f_{od0} \\ f_{od1} \\ f_{od2} \end{bmatrix} = \begin{bmatrix} -0.18 \\ 0.09 \\ -0.05 \end{bmatrix} \& \begin{bmatrix} f_{c0} \\ f_{c1} \\ f_{c2} \end{bmatrix} = \begin{bmatrix} -0.35 \\ 0 \\ 0 \end{bmatrix}$$
(29)

The CT $\Sigma\Delta M$ and its DT equivalent were simulated using Simulink[®]. The output spectrums of both modulators are plotted in Fig. 6, and the SNR (Signal-to-Noise Ratio) of both modulators are plotted versus the input amplitude in Fig. 7. It can be seen that there is a good agreement between the CT $\Sigma\Delta M$ and its DT equivalent.

IV. CONCLUSION

A generic and simple approach for designing CT $\Sigma\Delta M$ based on FIR DAC was introduced. The technique was further generalized to include FIR with half period delay and to modulators with delay compensation feedback branch. The numerical nature of the proposed technique, significantly simplifies the design, and increases the designer options. The technique was applied to a design example of a bandpass 4th order CT $\Sigma\Delta M$ based on LC filter, and the simulations showed a good agreement between the designed CT $\Sigma\Delta M$ and its DT equivalent.

References

- A. Ashry and H. Aboushady, "Using excess loop delay to simplify LCbased ΣΔ modulators," Electronics Letters, vol. 45, no. 25, pp. 1298– 1299, Dec. 2009.
- [2] O. Shoaei and W. Snelgrove, "Optimal (bandpass) continuous-time ΣΔ modulator," in *Proc. IEEE International Symposium on Circuits and Systems, (ISCAS'94)*, vol. 5, May 1994, pp. 489–492.
- [3] R. Schreier, "The delta-sigma toolbox for matlab," *Oregon State University*, Nov. 1999.
- [4] H. Aboushady and M. Louerat, "Systematic approach for discrete-time to continuous-time transformation of ΣΔ modulators," in *Proc. IEEE International Symposium on Circuits and Systems, (ISCAS'02)*, vol. 4, May 2002, pp. IV–229–232.
- [5] O. Shoaei and W. Snelgrove, "A multi-feedback design for lc bandpass delta-sigma modulators," in *Proc. IEEE International Symposium on Circuits and Systems, (ISCAS'95)*, vol. 1, May 1995, pp. 171–174.
- [6] B. K. Thandri and J. Silva-Martinez, "A 63 dB SNR, 75-mW Bandpass RF ΣΔ ADC at 950 MHz Using 3.8-GHz Clock in 0.25-μm SiGe BiCMOS Technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 269–279, Feb. 2007.
- [7] N. Beilleau, A. Kammoun, and H. Aboushady, "Systematic design method for lc bandpass sigma delta modulators with feedback firdacs," in *Proc. IEEE International Symposium on Circuits and Systems*, (ISCAS'06), Sept. 2006, pp. 1896–1899.
- [8] P. Benabes, M. Keramat, and R. Kielbasa, "A methodology for designing continuous-time sigma-delta modulators," in *Proc. European Design and Test Conference, (ED&TC'97)*, Mar. 1997, pp. 46–50.



Figure 5. Loop filter of the modulator.



Figure 6. Output Spectrum of the modulator output.



Figure 7. SNR of the modulator versus the input amplitude.