Systematic Design of Continuous-Time $\Sigma\Delta$ Modulator With VCO-Based Quantizer

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***Abstract*— A methodology for the design of Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulators with VCO-based quantizer is proposed. The coefficients of the CT $\Sigma\Delta$ modulator are accurately calculated such that the noise transfer function of the modulator is exactly the same as a Discrete-Time (DT) $\Sigma\Delta$ modulator of the same order. The proposed design method takes into account loop-delay compensation as well as the shape of the feedback Digital-to-Analog Converter (DAC) signal. VCO non-idealities such as non-linear K_{vco} and phase noise are studied. Several design examples for different modulator orders and feedback DAC signal shapes are given to validate the proposed methodology.**

I. Introduction

Modern wireless communication systems require high performance A/D converters with increasing bandwidth and resolution. Sigma-Delta modulators are usually used for high resolution while the use of multi-bit quantizers is necessary to maintain the high-resolution at wide-band operation [1] [2].

A Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulator with a VCO-based quantizer is shown in Fig. 1. Time domain quantizers, such as VCO-based [3] and integrator-based [4], emerge as potential candidates for modern CMOS technology due to the fact that they are less sensitive to supply voltage reduction compared to conventional voltage quantizers. The use of a VCO-based quantizer [3] [4] as a multi-bit quantizer inside the loop of a CT $\Sigma\Delta$ modulator reduces the total power consumption as well as the VCO non-idealities. This architecture is characterized by the abscence of power-hungry comparators, inherent Data Weighted Averaging (DWA) and additional noise shaping properties. The drawback of VCO-based quantizers is the limited input signal range due to VCO non-linearity.

In this work, a systematic method is proposed to calculate the coefficients of a CT $\Sigma\Delta$ modulator with VCO-based quantizer considering loop delay compensation [5]. This technique is based on the discrete-time to continuous-time (DT-CT) equivalence [6].

In section II, the VCO-based quantizer model is described. Section III presents the proposed methodology for discrete-time to continous-time transformation considering the VCO-based quantizer and the loop delay compensation. In section IV design examples are presented for several modulator orders and feedback DAC waveform shapes. System level and transistor level simulation results are presented for wide-band specifications. The conclusion is presented in section V.

[1]This work is partially funded by the French research project Nano2012 in cooperation with STMicroelectronics.

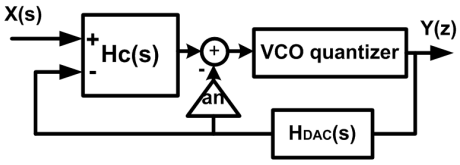

Fig. 1. Continuous-Time $\Sigma\Delta$ modulator with VCO-based quantizer.

II. VCO-quantizer model

VCO-based quantizers have different architectures and the one used in this work is shown in Fig.2. It requires a Ring-VCO, a set of standard registers, XOR gates, and an adder stage. The relative simplicity of the circuit is an important advantage for CT $\Sigma\Delta$ modulator allowing high speed operation with small latency. Metastability in this quantizer is a factor N less than a Flash quantizer where N is number of quantization levels. [7] The main idea is to count the number of inverters switching state within the clock period by comparing samples of their current and previous states. The inverters delay is set by the input tuning voltage. So the number of inverters switching state each clock period will represent the input tuning voltage and the total number of inverters (N) defines the quantizer resolution.

A Key constraint is that the maximum number of transitions in a clock period cannot exceed the total number of inverters [7]. This can also be expressed in terms of frequencies as

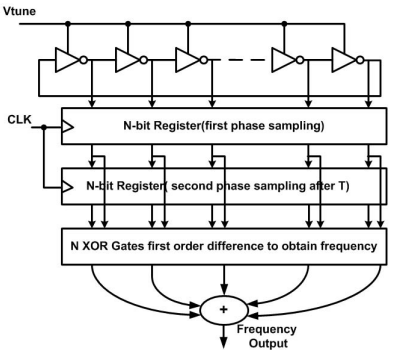

Fig. 2. VCO-based quantizer architecture.

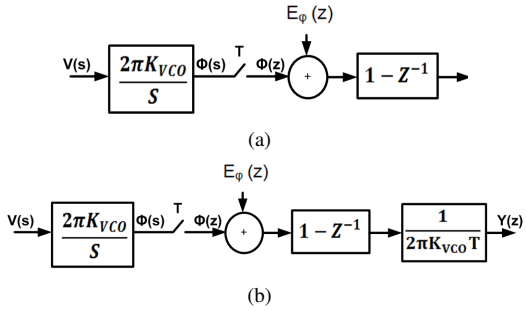

Fig. 3. (a) Linear model of a VCO-based quantizer (b) Linear model with frequency to voltage conversion

$$f_{vco,max} < \frac{fs}{2} \tag{1}$$

where f_{vco} is the vco output frequency and f_s is the sampling frequency.

Fig. 3(a) represents the linear model describing the architecture. The ring VCO is modeled as a CT integrator with gain $2\pi K_{vco}$. The Delay-Flipflops (DFF) are modeled as a sampler on the integrator output and the XOR operation is modeled as a discrete time differentiator. The output frequency f_{vco} representing the input voltage has to be converted back to voltage to feed the $\Sigma\Delta$ modulator DACs. Dividing by $2\pi K_{vco}T$ cancels the CT integrator gain and allows to insert the quantizer model in a CT $\Sigma\Delta$ modulator without changing its NTF, as will be explained in the following section. The required modification in the quantizer model is shown in Fig. 3(b). Moreover, the XOR outputs can be used to directly feed the DACs eliminating the need for a DWA dedicated ciruit which is usually used to linearize feedback multi-bit DACs This inherent property is advantageous in terms of area and power consumption.

III. Design methodology of CT $\Sigma\Delta$ with VCO-based quantizer

A. Applying DT-to-CT Transformation For CT $\Sigma\Delta$ With VCO-Based Quantizer

The discrete-time to continuous-time transformation [6] determines the coefficients of an N^{th} order CT $\Sigma\Delta$ modulator with the same Noise-Transfer-Function (NTF) of a DT $\Sigma\Delta$ modulator of the same order. This is done by comparing their respective loop gain transfer functions $G_c(z)$ and $G_d(z)$. For a DT $\Sigma\Delta$ modulator of a general order N, the corresponding $NTF_d(z)$ is

$$NTF_d(z) = \frac{1}{1 - G_d(z)} \tag{2}$$

The model of Fig.3 has to be rearranged to allow determining $NTF_c(z)$ with quantization noise represented in terms of voltage instead of phase. Then the $NTF_c(z)$ can be found combining the linear models of Fig.1 and Fig.4.

$$NTF_c(z) = \frac{Y(z)}{E_v(z)} = \frac{(1 - z^{-1})}{1 - G_c(z)} \tag{3}$$

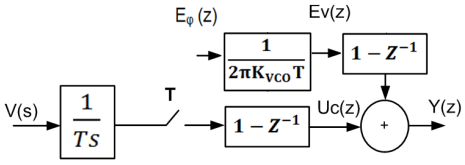

Fig. 4. Model with quantization noise converted from phase to Voltage.

$$G_c(z) = -(1 - z^{-1}) \times \mathcal{Z}\left\{H_{DAC}(s)(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts})\right\} \tag{4}$$

where T is the sampling period, $H_{DAC}(s)$ is the feedback DAC transfer function, $H_c(s)$ is the loop filter transfer function and a_n is the additional feedback coefficient. The inherent integration inside the quantizer requires this additional coefficient a_n to keep the NTF intact while having the same degrees of freedom for the modulator design.

In order to compare with (2), the $NTF_c(z)$ will be rewritten on the following form

$$NTF_c(z) = \frac{1}{1 - G_c'(z)} \tag{5}$$

$$G_c'(z) = -\frac{z^{-1}}{1 - z^{-1}} - \mathcal{Z}\left\{H_{DAC}(s)(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts})\right\} \tag{6}$$

Through symbolic equivalence between $G_c'(z)$ of (6) and $G_d(z)$ of (2), the coefficients of similar z orders are equated. Hence the CT $\Sigma\Delta$ modulator coefficients are determined considering the VCO-based quantizer and the equivalent NTF is the same as the DT $\Sigma\Delta$ modulator of the same order.

K_{vco} does not appear explicitly in the $NTF_c(z)$ of (5) and (6) but from Fig. 4 it can be shown that increasing K_{vco} should decrease the voltage quantization step and so the quantization noise will decrease without altering the $NTF_c(z)$. In consequence, the whole spectrum will be shifted down giving higher Signal-to-Noise-Ratio (SNR). [8].

B. Loop-Delay Compensation

Considering loop-delay from the quantizer and DACs, a fixed delay element is added as shown in Fig. 5 to mask this circuit dependent delay. Compensation coefficient is necessary to keep the NTF intact considering the added delay element.

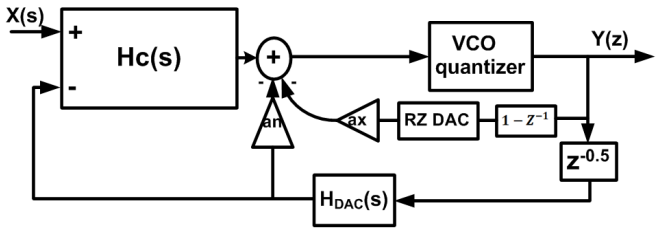

Fig. 5. CT $\Sigma\Delta$ modulator with VCO-based quantizer and loop delay compensation.

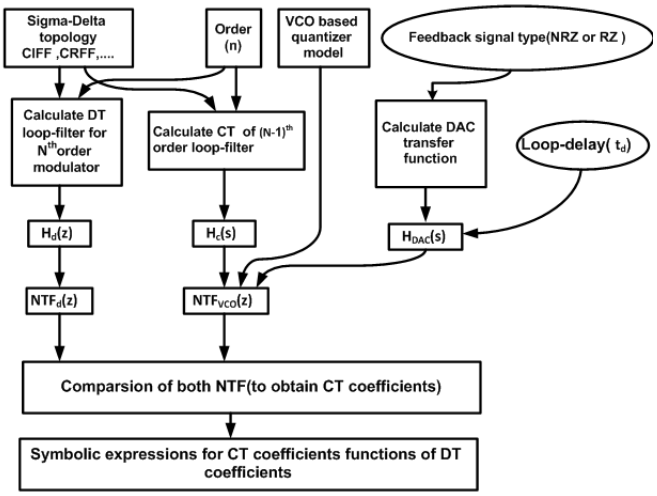

Fig. 6. The flowchart of the proposed systematic design methodology.

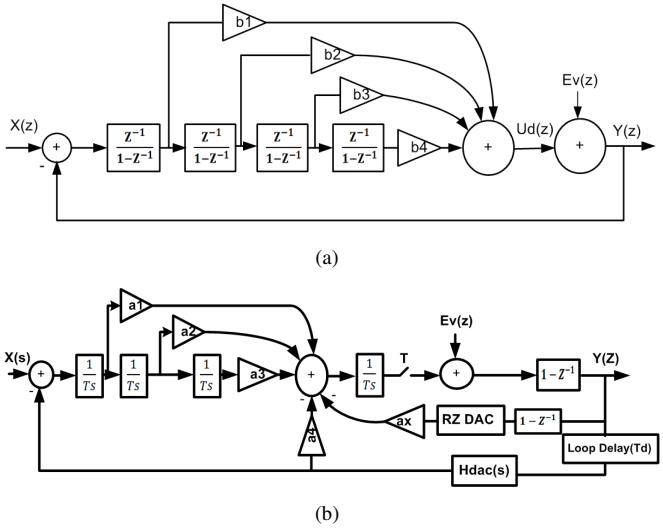

Fig. 7. 4^{th} order $\Sigma\Delta$ modulator CIFF (a) DT (b) CT

In a conventional $\Sigma\Delta$ modulator architecture, this additional feedback branch is substracted from the output of the last integrator and their difference is fed to the quantizer [5]. In this architecture, the last integration is inherent within the VCO and the substraction is not possible.

As shown in Fig. 5, the proposed solution is to add a discrete time differentiator in this branch in order to cancel the inevitable integration seen in this path. The use of a RZ DAC in this branch allows to mask the circuit delay without altering the modulator's NTF. This method should allow masking delays within $0.5T$ and the corresponding new loop gain $G_c^{''}(z)$ is given by (7)

$$G_c^{''}(z) = -\frac{z^{-1}}{1-z^{-1}} - z^{-0.5}\mathcal{Z}\left\{H_{DAC}(s)(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts})\right\}$$
$$-(1-z^{-1})\mathcal{Z}\left\{H_{RZ\,DAC}(s)\frac{a_x}{Ts}\right\} \quad (7)$$

Where $H_{RZ\,DAC}(s)$ is the RZ DAC transfer function and a_x is the added coefficient for compensating loop delay.

Symbolic equivalence is made between the new loop gain $G_c^{''}(z)$ of (7) and $G_d(z)$ of (2) to find the exact coefficients of a CT $\Sigma\Delta$ modulator with VCO-based quantizer of a general order while considering loop delay compensation. The proposed design methodology is summarized in Fig. 6.

IV. System Level Simulation Results

A. Design Example With Ideal VCO model

In order to verify the proposed design methodology, a 4^{th} order DT $\Sigma\Delta$ modulator with 4-bit quantizer is designed using Schreier Delta-Sigma toolbox [9] for the following wide-band specifications: OSR=16, bandwidth=20 MHz and f_s=640 MHz. The systematic design method presented in section III is used to get the equivalent CT $\Sigma\Delta$ modulator coefficients considering the VCO-based quantizer and the loop delay compensation. Fig. 7(a) shows the 4th order DT $\Sigma\Delta$ modulator linear model using a Cascade of Integrators in Feedforward (CIFF) architecture while the CT $\Sigma\Delta$ modulator equivalent model with VCO-based quantizer and loop delay compensation is shown in Fig. 7(b).

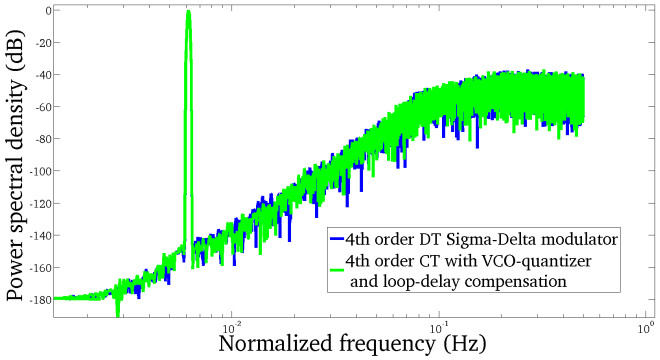

Fig. 8. The output Power Spectral Density for DT $\Sigma\Delta$ modulator and CT $\Sigma\Delta$ modulator with VCO-based quantizer and loop-delay compensation

The output power spectral density of the CT $\Sigma\Delta$ modulator is equivalent to that of the DT $\Sigma\Delta$ modulator shown in Fig. 8. The SNR plot versus the input amplitude in dB for both modulators is shown in Fig. 9. The results ensure that the CT $\Sigma\Delta$ modulator designed with the proposed method achieves a performance identical to the DT $\Sigma\Delta$ modulator of the same order. In order to verify the generality, SNR curves are traced and shown in Fig. 9 for other design examples such as 3^{rd} order $\Sigma\Delta$ modulator with resonator and 2^{nd} order $\Sigma\Delta$ modulator with RZ DAC. The curves traced from system level simulations verify the equivalence of DT and CT models.

B. VCO Phase Noise

Phase noise is added to the VCO model and CT $\Sigma\Delta$ modulator with VCO-based quantizer seems not to be limited by VCO phase noise even with an exagerated value of phase noise as -40 dBc at 1 MHz with input amplitude of -20 dB.

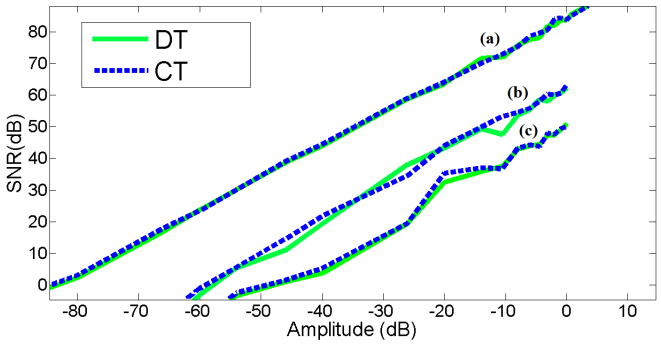

Fig. 9. SNR plot with input amplitude in dB for DT $\Sigma\Delta$ modulator and CT $\Sigma\Delta$ modulator with VCO-based quantizer and loop-delay compensation (a) 4^{th} order with loop delay compensation and NRZ DAC (b) 3^{rd} order with resonator and NRZ DAC (c) 2^{nd} order with RZ DAC

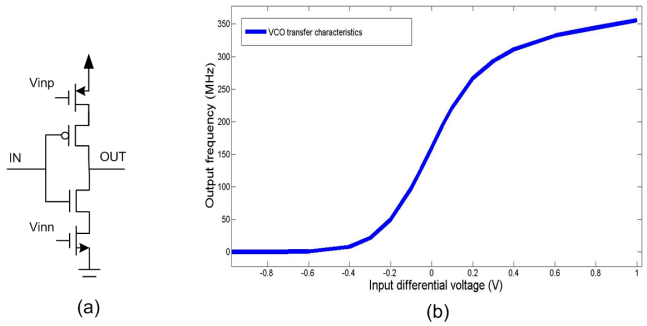

Fig. 10. (a) Single stage of the Ring VCO (b) VCO-transfer characteristics .

C. Transistor Level Simulation and VCO Non-linearity

As discussed in section IV-A, high values of K_{vco} allow higher quantizer resolution, thus higher SNR. Practically, K_{vco} is almost linear for small inputs while higher inputs give rise to harmonic distortion in the modulator output spectrum. Then, K_{vco} has to be chosen wisely to allow a suitable input range without increasing harmonic distortion. Fig. 10(a) shows a single stage of the ring VCO, while Fig. 10(b) illustrates the K_{vco} non-linear characterstics.

The VCO-based quantizer is described in transistor level using 0.13 μm CMOS technology. The integrators and DACs are ideally modeled. The maximum input range is -20 dB in order to achieve the target resolution with the presence of VCO non-linearities. The total delay of the XOR gates and the DFF is 0.34 ns $\approx \frac{T_s}{3}$. The output power spectral density from transistor level simulations of a VCO-based quantizer used within an ideal CT $\Sigma\Delta$ modulator are shown in Fig. 11. This figure compares the transistor level performance to the ideal performance with -20 dB input signal. The VCO non-linearity appears as a harmonic distortion in the output spectrum. Although the second and third harmonic are in band of interest, the total Signal-to-Noise-and-Distortion-Ration (SNDR) for this simulation is 74 dB with about 3dB loss with respect to the ideal model. Further investigation in VCO linearization techniques can lead to enhance the modulator dynamic range.

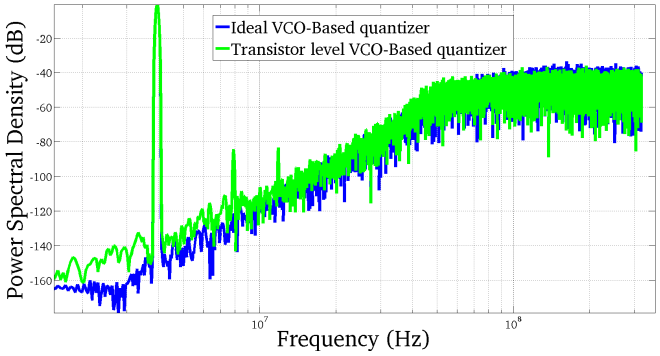

Fig. 11. Output power spectral density of a 4^{th} order CT $\Sigma\Delta$ modulator with VCO-quantizer on circuit-level with NRZ DAC.

Integrator-based quantizers [4] seem to remove the limitation on the input range and hence achieve higher SNDR in the same wide-band consuming more power.

V. Conclusion

In this paper, we presented a generalized method for the determination of the coefficients of CT $\Sigma\Delta$ modulator with VCO-based quantizer considering loop-delay. This method is general can be used for any modulator order with NRZ or RZ feedback DACs. Analysis for the VCO non-idealities are discussed and simulated and a design example is presented for a 4^{th} order modulator with 4-bit quantizer in 0.13 μm CMOS technology. VCO non-linearity which limits the input range, is the limiting factor for the maximum SNDR achieved.

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