A Mixed Equation-Based and Simulation-Based Design Methodology For Continuous-Time Sigma-Delta Modulators

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***Abstract*— This paper presents a design automation tool for continuous-time Sigma-Delta modulators from high level specifications down to Layout. System level synthesis, circuit synthesis as well as layout synthesis are performed in the CAIRO+ design environment. Strong interaction between the system level and the circuit level is used to optimize the final design. The design of a complete third order current-mode continuous-time Sigma-Delta modulator is taken as an example to show the effectiveness of the proposed design methodology.**

I. Introduction

Interesting work has been presented on the high level synthesis of Discrete-Time (DT) ΣΔ modulators for optimal topology selection and behavioral modeling of circuit non-idealities [1]. Top-down design methodologies from high level specifications down to layout for DT ΣΔ modulators have also been presented in [2][3]. Recently, Continuous-Time (CT) ΣΔ modulators are receiving increasing attention in high speed and low-power applications [4].

In this paper, we present a mixed equation-based and simulation-based design methodology for CT Sigma-Delta modulators from high level specifications down to Layout. The calculation and scaling of the Sigma-Delta coefficients as well as circuit sizing and layout generation are implemented in the same analog design environment CAIRO+. As can be seen from Figure 1, this has the important advantage to allow strong interaction between the different design levels. Here, we focus mainly on the interaction between the system-level and the circuit-level.

A mixed equation-based and simulation-based design methodology is used to implement the tool.

The paper is organized as follows. In Section II., system-level synthesis is presented. In section III., we present the circuit level design of the CT current-mode integrator, the current steering feedback DAC and the current comparator. Simulation-based circuit optimization is discussed in section IV.. Section V. is about layout synthesis. The conclusion is given in section VI..

II. System-level synthesis

A. Equation-based synthesis of CT ΣΔ coefficients

To calculate the coefficients of continuous-time ΣΔ modulators, we start from the coefficients of a DT ΣΔ modulator. Figures 2 and 3 show general forms of a CT ΣΔ modulator and its DAC feedback signal, respectively. The objective is to design the CT loop filter $H_c(s)$, for a given feedback DAC transfer function $H_{DAC}(s)$, so that the CT

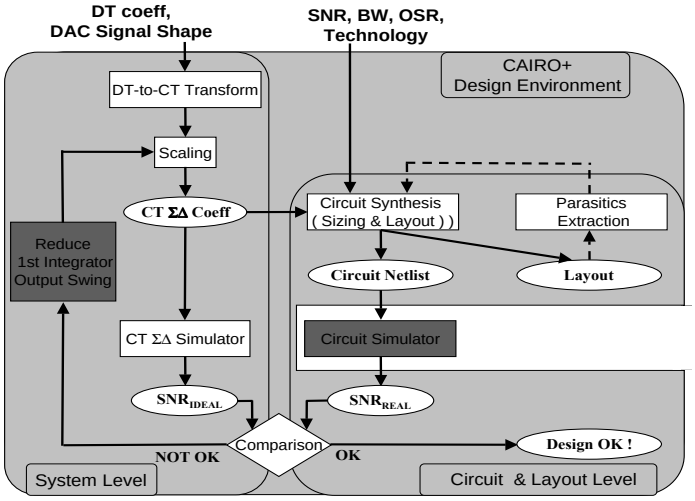

Fig. 1. CT ΣΔ modulator synthesis in the CAIRO+ design environment.

ΣΔ loop gain $G_c(z)$ is equal to the DT ΣΔ loop gain $G_d(z)$. This can be expressed by

$$\begin{aligned} G_d(z) &= G_c(z) \\ G_d(z) &= \mathcal{Z}\left[H_c(s)\ \ H_{DAC}(s)\right] \end{aligned} \tag{1}$$

A systematic technique for DT-to-CT transformation, based on the modified-z-transform technique, is then used to get the CT ΣΔ coefficients [5]. The complete procedure used to calculate the coefficients of a CT ΣΔ modulator, having an arbitrary feedback signal, is described in Figure 4. Using a symbolic mathematical tool, it is possible to obtain the CT coefficients $(a_1, a_2, \ldots, a_n)$ expressed in function of the DT coefficients $(b_1, b_2, \ldots, b_n)$ and the

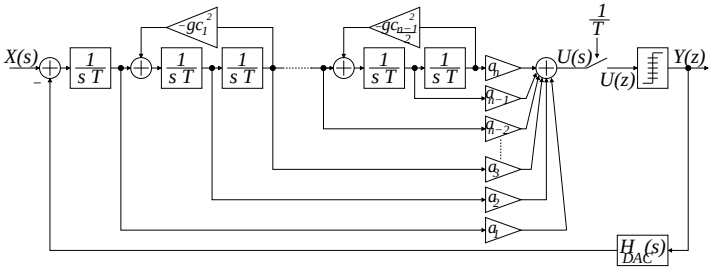

Fig. 2. General form of a continuous-time ΣΔ modulator.

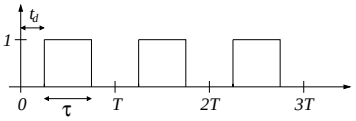

Fig. 3. Continuous-time rectangular feedback signal.

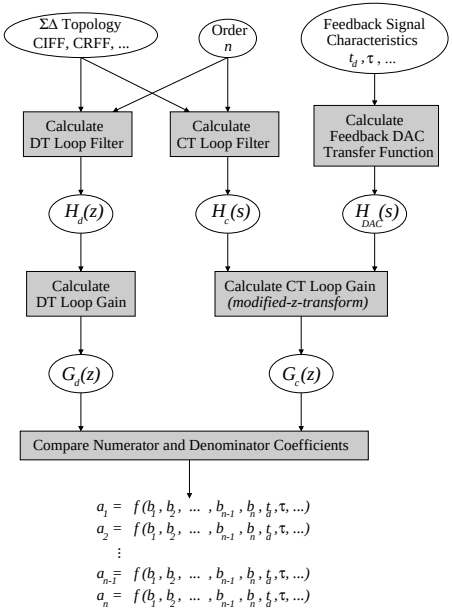

Fig. 4. Design procedure to find CT ΣΔ coefficients $(a_1, \ldots, a_n)$ in function of DT ΣΔ coefficients $(b_1, \ldots, b_n)$ and the feedback signal characteristics $(t_d, \tau, \ldots)$.

feedback signal characteristics $(t_d, \tau, \ldots)$:

$$\begin{aligned} a_1 &= f(b_1, b_2, \ldots, b_{n-1}, b_n, t_d, \tau, \ldots) \\ a_2 &= f(b_1, b_2, \ldots, b_{n-1}, b_n, t_d, \tau, \ldots) \\ &\vdots \\ a_{n-1} &= f(b_1, b_2, \ldots, b_{n-1}, b_n, t_d, \tau, \ldots) \\ a_n &= f(b_1, b_2, \ldots, b_{n-1}, b_n, t_d, \tau, \ldots) \end{aligned} \tag{2}$$

Symbolic DT-to-CT ΣΔ transformation tables are then obtained for different ΣΔ topologies, cascade of integrators or resonators in a feedforward or a feedback form.

B. Simulation-based scaling of CT ΣΔ coefficients

Since the ΣΔ modulators are non-linear systems, simulation is usually involved in the design procedure. In the CAIRO+ environment, functions have been developed in order to perform simulation of ideal CT ΣΔ modulators. Functions for Fast Fourier Transform (FFT) and Signal to Noise Ratio (SNR) calculation are also available for the analysis of the output signal.

The coefficients resulting from the DT-to-CT transformation tables, described in section A., ensure that both Noise Transfert Functions (NTF) of the DT and CT systems are identical. On the other hand, these coefficients do not take into account any circuit limitations. These coefficients do not ensure that the integrators outputs are

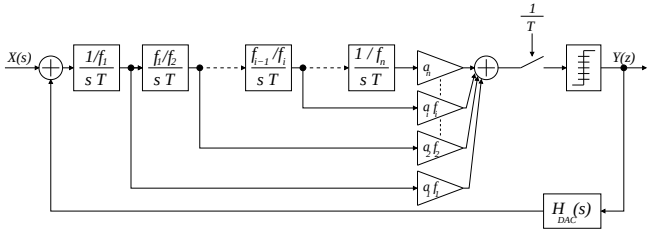

Fig. 5. Scaling factors are introduced to limit integrators output swing.

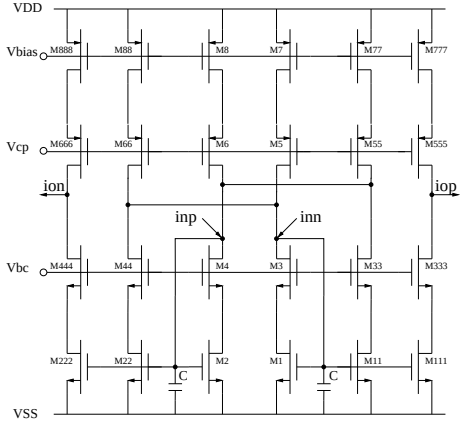

Fig. 6. The current-mode integrator.

limited to the maximum signal swing permitted by the circuit realizing the integrators. Due to the non-linearity of ΣΔ systems, the integrators output swing are difficult to predict mathematically and are then estimated by simulation. In [6], a systematic simulation-based technique to scale the CT ΣΔ coefficients for limited integrators output swing is presented. As seen in Figure 5, scaling factors $(f_1, f_2, \ldots, f_n)$ have been introduced to the CT ΣΔ system. These scaling factors are multiplied by the the CT ΣΔ coefficients and the integrators' gains in such a way that the NTF is kept unchanged. The starting value for all the integrators' gains and scaling factors is 1 and their final values will be determined by simulation using the following algorithm for an n^{th} order modulator:

1. the starting value for all the scaling factors is 1, $f_1 = f_2 = \ldots = f_n = 1$.
2. simulate the CT ΣΔ modulator with the previously determined scaling factor and the others left to 1, using a $-6dB$ sinusoidal input signal.
3. the scaling factor, f_i, corresponding to the i^{th} simulation is calculated using the following expression:

$$f_i = \frac{max(output\ i^{th}\ integrator)}{desired\ i^{th}\ integrator\ output\ swing} \tag{3}$$

4. repeat steps 2 and 3 until $i = n$

III. Equation-based circuit synthesis

In this section, the design procedures used to synthesize the integrator, the feedback DAC and the comparator of the continuous-time Sigma-Delta modulator are presented.
The biasing current and voltages are calculated using simplified MOS transistor models. The transistors' dimensions are then calculated using the accurate BSIM3v3 models implemented in CAIRO+.

A. Integrator Design Plan

Figure 6 shows the fully differential current-mode integrator, taken here as a design example. Neglecting output conductances and parasitic capacitances, and assuming identical transistors, small-signal analysis of this circuit yields the following transfer function:

$$H_{circuit}(s) = \frac{i_{inp}(s) - i_{inn}(s)}{i_{outp}(s) - i_{outn}(s)} = \frac{g_m}{s\,C} \tag{4}$$

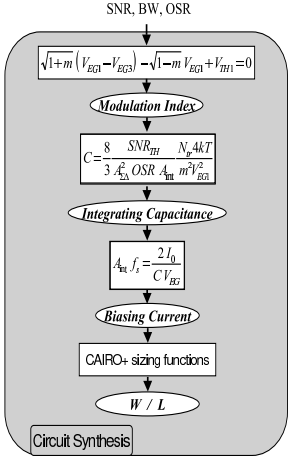

Fig. 7. Integrator synthesis procedure.

where g_m is the transconductance of the mirror transistors $M_1 - M_{111}$ and $M_2 - M_{222}$ and C is the integrating capacitance. Figure 7, shows the design procedure used to size the transistors of the current-mode integrator. It has been shown in [7], that the maximum modulation index, $m = \frac{I_{in}}{I_0}$, can be obtained using the following relation:

$$\sqrt{1+m}\,(V_{EG_1} + V_{EG_3}) - \sqrt{1-m}\,V_{EG_1} - V_{TH_1} = 0 \quad (5)$$

where V_{EG_1} and V_{EG_3} are the effective gate voltages of the mirror transistor M_1 and the cascode transitor M_3, respectively.

The minimum integrating capacitance, C, necessary to achieve the desired SNR is calculated using the following equation [7]:

$$C = \frac{8}{3}\,\frac{SNR}{A_{\Sigma\Delta}^2\,OSR\,A_{int}}\,\frac{N_{tr}\;4KT}{m^2\,V_{EG_1}^2} \quad (6)$$

the integrator gain, A_{int}, and the input signal gain for maximum SNR, $A_{\Sigma\Delta}$, are parameters calculated during the system level design. N_{tr} is the number of transistors contributing noise.

The transfer function of each integrator in the $\Sigma\Delta$ modulator is determined during the system level design. This transfer function can be written in the following form

$$H_{system}(s) = \frac{A_{int}}{s\,T} \quad (7)$$

Comparing (7) and (4), it is obvious that for proper operation of the modulator the following relation must be satisfied:

$$A_{int}\;f_s = \frac{g_m}{C} \quad (8)$$

where $f_s = \frac{1}{T}$ is the sampling frequency of the modulator. The transconductance g_m can also be written in the following form

$$g_m = \frac{2\;I_0}{V_{EG}} \quad (9)$$

By substitution from equation (9) into equation (8) we find that

$$A_{int}\;f_s = \frac{2\;I_0}{V_{EG}\;C} \quad (10)$$

Equation (10) is then used to calculated the biasing current I_0 of the integrator. Using the BSIM3v3 sizing functions, we can generate a complete sized netlist of the integrator.

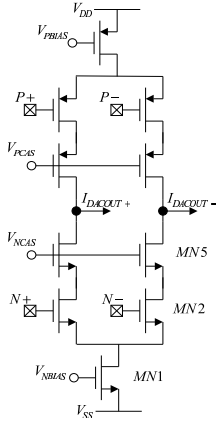

Fig. 8. DAC circuit.

This integrator satisfies the required Signal-to-Thermal Noise ratio. On the other hand, this sizing procedure does not take the non-linearity of the integrator into account. The main source of harmonic distortion in the current-mode integrator, shown in Figure 6, is g_m variation with the input current. It is possible to find an approximate expression for the transconductance $g_m(t)$ in function of the nominal transconductance g_{m_0}, the input current $i_{in}(t)$, the biasing current I_0 and the integrator gain A_{int}:

$$g_m(t) = g_{m_0}\sqrt{1 + \frac{A_{int}}{I_0}\frac{1}{T}\int_0^t i_{in}(t)\;dt} \quad (11)$$

From equation (11), we can see that it is possible to reduce the transconductance nonlinearity either by increasing the biasing current I_0 or by decreasing the integrator gain A_{int}. In a low-power design, it is preferable to decrease the integrator gain A_{int}. If A_{int} is changed, all the coefficients of the $\Sigma\Delta$ modulator must be scaled in order to preserve the same NTF.
Note that, although equation (11) is useful to identify the design parameters that influence the non-linearity of the integrator, it is very difficult to use this equation to estimate harmonic distortion of the CT $\Sigma\Delta$ modulator.

B. Feedback DAC Design Plan

Figure 8 shows the Feedback DAC circuit. Transistor MN_1 acts as a current source and must be biased in deep saturation. Transistor MN_2 acts as a switch and is biased in the linear region. MN_5 is a cascode transistor biased in the saturation region.
The biasing current I_{DAC_i} is calculated in function of the integrator biasing current I_{bias} and the feedback coefficient, $coef_i$, using the following relation:

$$I_{DAC_i} = \frac{1}{2}\;m\;I_{bias}\;coef_i \quad (12)$$

Note the biasing voltages, should be given in function of the supply voltage or in function of other biasing voltages. This renders the design procedure independent from the technology and the desired specifications.
Using the above information, the BSIM3v3 sizing functions are able to calculate the exact value of each transistor width.

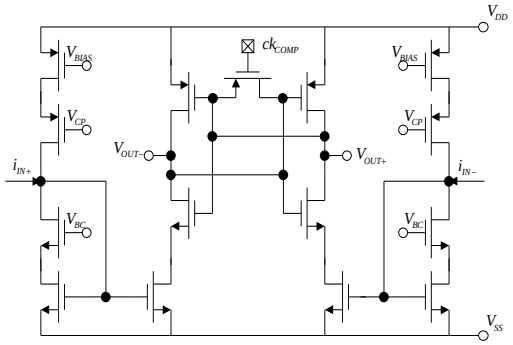

Fig. 9. Current-mode comparator.

C. Comparator Design Plan

The current-mode comparator circuit is depicted in Figure 9. At its inputs, current mirrors, biased with the same current as the third integrator, copy the input signal to a clocked CMOS cross-coupled latch.

IV. Simulation-based optimization

Circuit simulation is used to measure harmonic distortion due to the non-linearity of the integrator circuit. The simulated circuit consists of a CT $\Sigma\Delta$ modulator using the sized netlist of the integrator (section A.) along with ideal models for the comparator and the feedback DAC. FFT_{REAL} and SNR_{REAL} calculations are performed on the simulation output. The CT $\Sigma\Delta$ simulator described in section B. is used to obtain FFT_{IDEAL} and SNR_{IDEAL}. The results of the system level simulation and circuit level simulation are compared.

If $SNR_{REAL} < SNR_{IDEAL}$, the gain of the 1st integrator is reduced and the remaining coefficients are scaled in order to maintain the same NTF. Another circuit is then generated for the new coefficients. These steps are repeated until the difference between SNR_{REAL} and SNR_{IDEAL} is small. This optimization procedure is described in Figure 1.

Figure 10 shows the results of such an optimization for a third-order continuous-time $\Sigma\Delta$ modulator. We can clearly see the large amplitude of the third harmonic for the first simulation done with coefficients scaled for maximum signal swing ($A_{int_1} = 0.216$). After several iterations, we find a suitable value ($A_{int_1} = 0.043$) which attenuates the third harmonic and gives an SNR_{REAL} very close to SNR_{IDEAL}.

The main drawback of decreasing A_{int} is the corresponding increase in the integrating capacitance.

V. Layout Synthesis

In order follow a layout-aware approach for circuit synthesis [8], it is compulsory to be able to predict parasitics resulting from layout, early in the synthesis phase. Thus, we have chosen an approach using layout templates with dedicated layout device generators. The layout template which describes the relative placement of instances inside a circuit, is designed with the CAIRO+ language [9]. Device generators are available to the designer in the CAIRO+ environment. They can provide two types of information : layout and electrical information taking into account layout parasitics. These generators allow a given schematic to be ported to a new process or a new set of specifications.

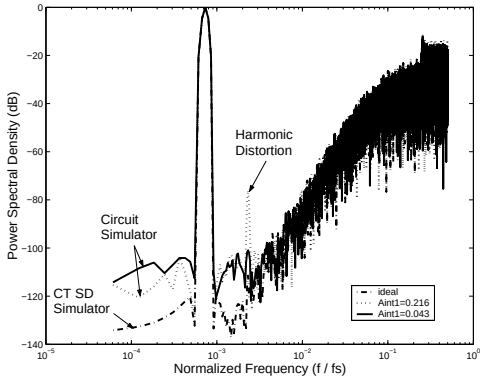

Fig. 10. Comparison between ideal system-level $\Sigma\Delta$ simulation and circuit level simulation.

VI. Conclusion

A top-down design methodology of continuous-time $\Sigma\Delta$ modulators has been presented. The design methodology is mainly equation-based.

Simulation is used in the system level to scale the calculated CT coefficients. In the circuit level, simulation is used to estimate harmonic distortion.

It has been shown that circuit non-linearity can be reduced only by modifying the CT $\Sigma\Delta$ coefficients and without increasing the power consumption. Having almost all the calculations and simulations integrated in the same design environment, permitted strong interaction and optimization between the different design levels.

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